CHAPTER 4 - RELIABILITY TESTS AND RELIABILITY PREDICTION

4

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4.1 Approach Toward Reliability 120

4.2 What are Reliability Tests 121

4.2.1 Reliability Test Significance and Purpose 121

4.2.2 Reliability Test Methods 121

4.2.3 Failure Criteria 126

4.3 Accelerated Life Tests 127

4.3.1 Purpose of Accelerated Life Tests 127

4.3.2 Acceleration by Temperature 127

4.3.3 Acceleration by Temperature and Humidity 128

4.3.4 Acceleration by Voltage 128

4.3.5 Acceleration by Temperature Difference 129

4.4 Reliability Evaluation by TEG 130

4.4.1 Test Element Group (TEG) 130

4.4.2 TEG for Reliability Evaluation 130

4.4.2.1 Process TEG 130

4.4.2.2 Circuit TEG 131

4.4.2.3 Bipolar Discrete TEG 131

4.4.2.4 Package Evaluation TEG 132

4.4.3 Reliability Evaluation Methods Using TEG 134

4.4.3.1 Wafer Level Reliability (WLR) 134

4.5 Reliability Prediction 136

4.5.1 Semiconductor Device Failure Rate 136

4.5.1.1 Semiconductor Device Failure Regions 136

4.5.1.2 Initial Failures 137

4.5.1.3 Random Failures 139

4.5.1.4 Wear-out Failures 140

4.5.2 Acceleration Theory 141

4.5.3 Stress Acceleration Tests 143

4.5.4 Failure Rate Prediction Case Studies 144

4.6 Test Coverage 151

4.7 Reliability Related Standards 152

4.1 Approach Toward Reliability

With recent advances in the systematization, functions and performance of equipment, the social impact and damages produced by failures are increasing, and high reliability has come to be demanded of equipment. This means that even higher reliability is demanded of the individual components which comprise equipment. Large quantities of semiconductors are used in a single piece of equipment, and these semiconductors often handle the main functions of that equipment, so high reliability is extremely important.

Semiconductors themselves are also becoming more miniaturized and highly integrated, with larger-scale circuit configurations. In addition, as semiconductor functions and performance advance and evolve into system LSIs, ensuring semiconductor reliability has become a vital matter.

The failure rate is often used as a general index for representing semiconductor reliability.

Semiconductor failure rates have been said to trend as shown in Fig. 4-1. This graph shape resembles a bathtub, so it is called a bathtub curve. In addition, failures have been classified into the three regions of initial failures, random failures and wear-out failures according to the time of occurrence.

Initial failures:

These are failures which occur at a relatively early time after the start of use.

These failures are characterized by a decrease in the failure rate over time.

The main causes of initial failures are manufacturing or material defects.

Random failures:

These failures are said to occur at a fairly constant failure rate after the initial failure period until wear-out failures occur.

With the exception of software errors described hereafter, intrinsic random failures are often thought not to exist.

Wear-out failures:

These are failures caused by wear and fatigue, and occur due to the physical limits of the materials which comprise semiconductor devices.

The failure rate increases with time, and these failures are used to determine the life.

However, the thinking that intrinsic random failures do not exist is changing recently.

That is to say, intrinsically only initial and wear-out failures exist as shown in Fig. 4-2, and the period between the two is comprised of the fringes of each failure distribution. This approach states that the failure rate during this intermediate period can be reduced by carrying out improvements for initial and wear-out failure factors.

The Sony Semiconductor Network Company also places emphasis on initial and wear-out failures in semiconductor reliability.

Initial failure rate levels are confirmed during development and design, and screening conditions are set as necessary to prevent defective products from escaping to the market.

In addition, semiconductor products are checked using accelerated tests to ensure that they have sufficient life so that wear-out failures do not occur during the normal usage period.

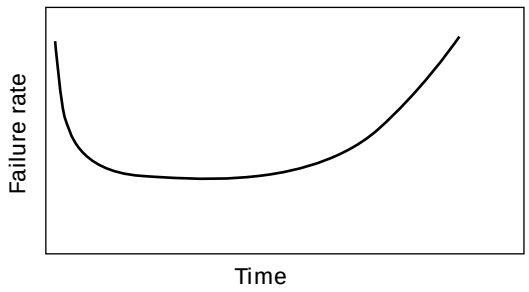


Fig. 4-1 Conventional Bathtub Curve

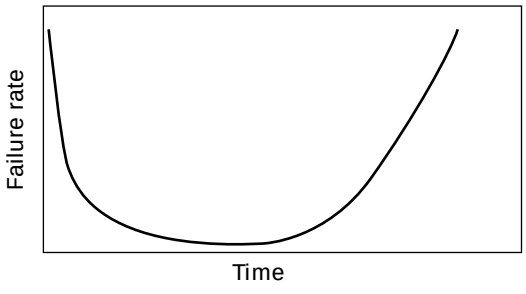


Fig. 4-2 Bathtub Curve Excluding Random Failures

4.2 What are Reliability Tests

4.2.1 Reliability Test Significance and Purpose

As defined under JIS Z 8115 (Reliability Terminology), “Reliability Test” is the general term for reliability determination tests and reliability compliance tests. In other words, reliability characteristics values (failure rate, reliability, average life, MTTF, etc.), which are scales representing the time-dependent quality of products, are estimated and verified statistically from the test data. These tests also play an important role in improving reliability by analyzing failures which occur during tests and clarifying these failure mechanisms. Reliability tests provide the greatest effects when statistics and failure physics function reciprocally.

Specific purposes of reliability tests are as follows.

(1) Product reliability assurance
(2) Evaluating new designs, components, processes and materials
(3) Investigating test methods
(4) Discovering problems with safety
(5) Accident countermeasures
(6) Determining failure distributions
(7) Collecting reliability data
(8) Reliability control

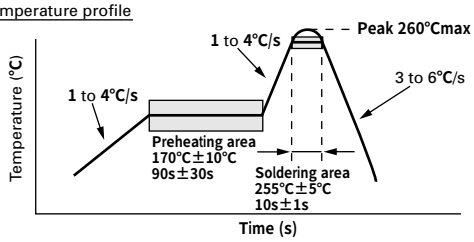
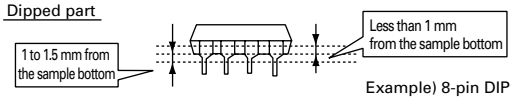
In addition, reliability tests are classified under various names according to the test format, purpose, method of applying stress, and other factors.

4.2.2 Reliability Test Methods

Reliability test items, conditions and other factors are determined based on customer needs for reliability, by clarifying the environmental and time conditions under which devices will be used and the failure definitions. It is also important to select test methods which are as standardized as possible in consideration of test reproducibility, cost effectiveness, data compatibility and other factors. The Sony Semiconductor Network Company has carried out tests centering on the JIS and MIL standards, and also performs reliability tests which support EIAJ, JEDEC and other standards as well.

Table 4-1 shows examples of standard reliability test items and methods used by the Sony Semiconductor Network Company.

Table 4-1 List of Standard Reliability Tests (IC) 1/5

<table>
<tr><th>Test item</th><th>Conditions</th><th>Failure criteria</th><th>Standard time</th></tr>
<tr><td>Soldering heat resistance [SMD]</td><td>Method 1: Solder bath dipping method at 260 ± 2°C
Method 2: Infrared reflow heating method at 260°Cmax
• Perform baking and moisture absorption at each of the conditions prescribed in the individual standards before heating.
The time from baking to moisture absorption shall be 5 minutes or less, and the time from moisture absorption to reflow or solder dipping shall be 2 hours or less.
• In method 1, solder dip the entire sample one time.
• The dipping time for method 1 shall be 10 ± 1 s.
• In method 1, perform flux dipping before solder dipping. (using rosin-based active flux)
• In method 2, heating shall be performed three times as standard based on the reflow temperature profile prescribed in the individual standards.
[Baking → moisture absorption → heating → heating → heating]
• In method 2, place the sample on a dedicated ceramic holder for heating.
Temperature profile
 
</td><td>Significant delamination shall not be confirmed through scanning acoustic tomography.
External and internal cracking shall not be confirmed through external visual inspection and cross section polishing inspection.
Failures shall not occur in continued reliability tests.</td><td></td></tr>
<tr><td>Soldering heat resistance [non-SMD]</td><td>Solder dip the prescribed part of the sample according to any one of the following methods.
<table><tr><th></th><th>Solder temperature [°C]</th><th>Dipping time [s]</th></tr><tr><td rowspan="2">Lead dipping only</td><td>260 ± 2°C</td><td>10 ± 1</td></tr><tr><td>350 ± 10°C</td><td>3.5 ± 0.5 ∗</td></tr><tr><td>Dipping to package bottom</td><td>260 ± 2°C</td><td>10 ± 1</td></tr></table>Dipped part
 

Example) 8-pin DIP
• The soldering iron may directly contact the sample pins. (∗)
• Dip the sample in rosin-based flux (active) before solder dipping.
• There is no particular need for moisturizing.</td><td>The electrical characteristics prescribed in the individual specifications shall be satisfied.</td><td></td></tr>
</table>

Table 4-1 List of Standard Reliability Tests (IC) 2/5

Test item	Conditions	Failure criteria	Standard time
High temperature bias (HTB)	Set the sample to the prescribed operating status under the following high temperatures. [Ambient temperature] A : 150 ± 5℃ B : 125 ± 5℃ • High temperature operation circuits (figure) shall be prescribed individually. • The ambient temperature shall be prescribed separately when the junction temperature (Tj) exceeds the rated value. • The preconditions shall be prescribed individually when necessary.	The electrical characteristics prescribed in the individual specifications shall be satisfied.	1000h
Low temperature bias (LTB)	Set the sample to the prescribed operating status under the following low temperature. [Ambient temperature] –65 ± 5℃ • Low temperature operation circuits (figure) shall be prescribed individually. • The preconditions shall be prescribed individually when necessary.	The electrical characteristics prescribed in the individual specifications shall be satisfied.	1000h
Temperature humidity bias (THB)	After performing the soldering heat resistance test as the preconditions, continue and supply power to the sample under the following high temperature and high humidity. Temperature [℃] | 85 ± 3 Humidity [%RH] | 85 ± 5 • The power-on (bias) circuits (figure) shall be prescribed individually. • Select intermittent power-on (1 h: ON/3 h: OFF) or continuous power-on according to the amount of heat generated by the sample.	The electrical characteristics prescribed in the individual specifications shall be satisfied.	1000h
Pressure Cooker Test (PCT)	After performing the soldering heat resistance test as the preconditions, continue and expose the sample to the following high temperature, high humidity and high pressure. Temperature [℃] | 121 ± 3 Humidity [%RH] | 100^{+0}_{-3} Vapor pressure [Pa] | $2.03 \times 10^5 \pm 10\%$	The electrical characteristics prescribed in the individual specifications shall be satisfied.	96h
Highly-accelerated temperature and humidity stress test (HAST)	After performing the soldering heat resistance test as the preconditions, continue and supply power to the sample under the following high temperature, high humidity and high pressure. Temperature [℃] | 130 ± 5 Humidity [%RH] | 85 ± 5 Vapor pressure [Pa] | $2.3 \times 10^5 \pm 10\%$ • The power-on (bias) circuits (figure) shall be prescribed individually.	The electrical characteristics prescribed in the individual specifications shall be satisfied.	

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Table 4-1 List of Standard Reliability Tests (IC) 3/5

<table>
<tr><th>Test item</th><th>Conditions</th><th>Failure criteria</th><th>Standard time</th></tr>
<tr><td>Thermal shock (TS)</td><td>After performing the soldering heat resistance test as the preconditions, continue and perform this test.
Repeatedly subject the sample to sudden temperature changes in the liquid phase as shown in the table below.
<table><tr><td>Order</td><td>1</td><td>2</td></tr><tr><td></td><td>–65 ± 5°C</td><td>150 ± 5°C</td></tr><tr><td>Time [min]</td><td>5</td><td>5</td></tr></table>• Start from room temperature to the low temperature side.
• The temperature transition time shall be 10 s or less.
• The medium shall be Perfluoropolyether (GALDEN®).
[Electronics test grade D02 TS]</td><td>The electrical characteristics prescribed in the individual specifications shall be satisfied.</td><td>100 cycles</td></tr>
<tr><td rowspan="3">Temperature cycle (TC)</td><td>After performing the soldering heat resistance test as the preconditions, continue and perform this test.
Repeatedly subject the sample to sudden temperature changes in the gaseous phase as shown in the table below.
1) Plastic molded packages
<table><tr><td>Order</td><td>1</td><td>2</td><td>3</td><td>4</td></tr><tr><td></td><td>–65 ± 5°C</td><td>Room temperature</td><td>150 ± 5°C</td><td>Room temperature</td></tr><tr><td>Time [min]</td><td>30</td><td>5^{+0}_{-1}</td><td>30</td><td>5^{+0}_{-1}</td></tr></table>• Room temperature here indicates 25 ± 15 °C.</td><td>The electrical characteristics prescribed in the individual specifications shall be satisfied.</td><td>100 cycles</td></tr>
<tr><td>2) Flip chips and chip size packages (CSP)
<table><tr><td>Order</td><td>1</td><td>2</td></tr><tr><td></td><td>–25 ± 5°C</td><td>125 ± 5°C</td></tr><tr><td>Time [min]</td><td>10</td><td>10</td></tr></table>Note) For flip chips and CSP, the prescribed temperature shall be the sample surface temperature (T_s). For other conditions, the prescribed temperature shall be the temperature inside the test tank near the blow-off opening (T_a).</td><td>The electrical characteristics prescribed in the individual specifications shall be satisfied.</td><td></td></tr>
<tr><td>3) Ball grid arrays (BGA)
<table><tr><td>Order</td><td>1</td><td>2</td></tr><tr><td></td><td>0 ± 3°C</td><td>125 ± 5°C</td></tr><tr><td>Time [min]</td><td>15</td><td>15</td></tr></table></td><td>The electrical characteristics prescribed in the individual specifications shall be satisfied.</td><td></td></tr>
</table>

Table 4-1 List of Standard Reliability Tests (IC)

Test item	Conditions	Failure criteria	Standard time
Lead strength	1) Tensile strength Apply the prescribed tensile force in the pin lead-out axial direction for 10 ± 1 s. • This test does not apply to packages with J-shaped leads or lead-less packages. • The load value shall be prescribed separately according to the pin cross-sectional area and wire diameter.	There shall be no pin severance, breakage or other mechanical damage.	
	2) Bending strength Hold the sample so that the pin lead-out axis is vertical, and attach the prescribed load to the tip of the pin. Rotate the sample 90° and then return it to the original position over a period of 2 to 3 s. Count this as one time. Next, rotate the sample at the same speed so that the lead pin is facing 90° in the opposite direction (in the same direction for flat pins), and then return it to the original position. Count this as the second time. • The load value shall be prescribed separately according to the pin cross-sectional area and wire diameter. • This test shall be performed two times. • The bending test shall not apply to SMD. • The twisting strength test is not prescribed.	There shall be no pin severance, breakage or other mechanical damage.	
Solderability	Dip the sample pins into a solder bath and visually judge (up to 30 × magnification) the degree of solder adhesion to the judgment portion. Solder plated → S-Pd PPF* Solder temperature → Sn/Pb : 230°C for 3 s; Sn/Ag/Cu: 245°C for 3 s Dipping time → 3 ± 0.5 Preconditions → 105°C100%RH 4h • The valid judgment portion shall be prescribed individually for each pin shape. *Sony specification palladium PPF	95% or more of the judgment portion shall be smoothly covered with solder, and pinholes, voids and other defects shall not be clustered in a single location or exceed 5% of the entire judgment area.	
Electrostatic strength	1) Machine Model (C = 200 pF, R = 0 Ω) • The number of applications shall be 1 time each, and the discharge current waveform shall be prescribed separately.	According to the individual specifications.	
	2) Human Body Model (C = 100 pF, R = 1.5 kΩ) • The number of applications shall be 3 times. • The discharge current waveform shall be prescribed separately.	According to the individual specifications.	
	3) Charged Device Model Maintain the potential of all the sample pins at the test voltage value via resistors, then contact the pin to be tested to a discharging metal object to discharge the pin. Carry out this procedure for each test pin. • All sample pins shall be tested. • The number of discharges shall be one time per test pin. • The discharge current waveform shall be prescribed separately.	According to the individual specifications.	

Table 4-1 List of Standard Reliability Tests (IC) 5/5

Test item	Conditions	Failure criteria	Standard time
Latch-up	1) Pulse current injection method Apply the supply voltage to the sample, fix the input pins to high or low, leave the output pins open, and then apply the prescribed constant current pulse to the test pin. Measure the supply current fluctuation at this time to determine whether latch-up has occurred. • The trigger pulse current waveform shall be prescribed separately. • The latch-up failure criteria current value shall be prescribed individually. • The tested pins shall be all pins other than power supply, GND and NC pins. • The trigger pulse shall be applied one time per test current value.	According to the individual specifications.	
	2) Power supply overvoltage method Apply the supply voltage to the sample, fix the input pins to high or low, leave the output pins open, and then raise the supply voltage value to the trigger pulse voltage value. Measure the supply current fluctuation at this time to determine whether latch-up has occurred. • The trigger pulse shall be applied one time. • The latch-up failure criteria current value shall be prescribed individually. • The trigger pulse voltage waveform shall be prescribed separately.	According to the individual specifications.	

4.2.3 Failure Criteria

When attempting to handle reliability characteristics values in a quantitative manner, it is important to clearly prescribe the operating environment and time-dependent conditions and the failure mode.

Conditions such as complete function failure or loss of important functions are generally easily clarified, but quantitative standards must also be set for drops in output, function deterioration and other failures occurring as gradual changes over time. In addition, failure criteria must take into account possible differences due to product users and customers.

The Sony Semiconductor Network Company states that in principle, electrical characteristics should be within the basic standard value range prescribed individually in the specifications for each product.

In this case, appropriate margins are set in the standard values themselves, so these do not indicate limit values at which products will absolutely fail as soon as these values are deviated from during actual use. In addition to standard values, there are also criteria which focus on the rate of change from the initial value. However, both types of criteria are set to detect changes and deterioration trends at an early stage, and to increase test efficiency. Table 4-2 shows example failure criteria for variable capacity diodes which are discrete semiconductors.

Table 4-2 Example Failure Criteria

Item	Measurement conditions	Specification	Failure criteria
I_R (Leak current)	V_R = 28V	10 nA or less	USL×2 (Upper limit)
V_F (Forward voltage)	I_F = 10mA	———	IVD×1.30
V_R (Reverse voltage)	I_R = 500 A	30 V or more	|IVD|×1.20

USL: Upper Specification Limit IVD: Initial value

4.3 Accelerated Life Tests

4.3.1 Purpose of Accelerated Life Tests

Innovations in semiconductor process technology are advancing at a blinding pace in recent years. Furthermore, given recent demands for shorter product development times, product reliability has been placed in the same situation as product development, and reliability characteristics must also be understood in a short time.

Based on these circumstances, accelerated life tests are methods for understanding reliability with the minimum sample size and the shortest test time. The JIS standard defines “accelerated tests” as “tests carried out under conditions more severe than standard conditions for the purpose of shortening the test time.”

Conducting tests under these severe conditions makes it possible to predict market failure rates in a short time using few samples, thus reducing both the time and cost required to confirm reliability.

4.3.2 Acceleration by Temperature

Semiconductor life is extremely sensitive to temperature, so life acceleration by temperature is almost always used as an accelerated test.

This temperature stress-based reaction was standardized by Arrhenius, and the Arrhenius model is widely used to predict semiconductor product life.

This Arrhenius model formula is expressed as follows.

$$\tau = A \cdot \exp\left(\frac{Ea}{kT}\right)$$

Where,
τ : Life
Ea : Activation energy (eV)
T : Absolute temperature (K)
A : Constant
k : Boltzmann’s constant

The above formula shows that semiconductor life depends on the temperature to which the semiconductor is exposed. Accelerated tests which utilize this characteristic are called temperature acceleration tests.

However, some failures such as those caused by hot carrier effects (the phenomenon where high energy carriers generated by electric fields are captured by the gate oxide film) may have negative activation energy values. When accelerating these types of failures, the test effectiveness increases as the test temperature is reduced.

4.3.3 Acceleration by Temperature and Humidity

LSI are tested under high temperature and high humidity environments to understand semiconductor life when exposed to high temperature and high humidity.

The high temperature and high humidity bias test, pressure cooker test, highly-accelerated temperature and humidity stress test (HAST), etc. are generally used as accelerated tests for humidity.

Humidity is rarely applied as the sole accelerating factor to confirm moisture resistance, and instead a combination of temperature and humidity stress is generally applied. This is done to promote the reaction to humidity (water), and leads to increased acceleration of the humidity life.

The general formula for humidity-related life is expressed as follows.

$$\tau = A \cdot P_{H_2O}^{-n}$$

Where,
τ : Life A, n : Constants

There is still no standardized formula for humidity-related life, and each manufacturer evaluates accelerated life using their own characteristic constants.

Particularly with humidity acceleration, increasing the relative humidity to around 100% for acceleration purposes may cause condensation to form on the sample, making it impossible to determine the original moisture resistance life. Therefore, sufficient care must be given to temperature and humidity control.

4.3.4 Acceleration by Voltage

Voltage acceleration tests differ greatly according to the device characteristics (MOS, bipolar and other processes, and circuit configuration).

Voltage acceleration tests are said to be effective for MOS LSI, and are often used to evaluate the resistance of gate oxide films. However, voltage acceleration is said to be difficult for bipolar LSI. The voltage acceleration life is expressed as follows.

$$\tau = A \cdot \exp(-V \cdot \beta)$$

Where,
τ : Life A, β : Constants V : Voltage

4.3.5 Acceleration by Temperature Difference

Semiconductors are comprised of combinations of various materials, and the coefficients of thermal expansion of these materials also vary widely. The difference between the coefficient of thermal expansion of each material causes damage (internal force) to accumulate (or sudden breakdown) each time the device experiences a temperature difference, which may lead to eventual failure. Accelerated tests based on temperature differences are carried out to understand this life.

Temperature cycle tests which apply a greater temperature difference than those normally experienced by the device are effective as accelerated tests for evaluating damage caused by temperature differences. Temperature cycle tests refer to tests used to evaluate the device resistance when exposed to high and low temperatures, and also the resistance when exposed to temperature changes between these two temperature extremes. These tests allow confirmation of semiconductor product resistance to temperature stress in the market (for example, the temperature change experienced by a device mounted or left inside an automobile from daytime to nighttime, or when a device cools from high temperature due to self heating when the power is on to room temperature when the power is turned off).

Life related to these temperature differences has been modeled by Coffin-Manson, and is expressed as follows.

$$\tau = A(\Delta T)^m$$

Where,
τ : Life A, m : Constants

This formula shows that accelerated tests can be established for temperature cycle life by providing a large ΔT (temperature difference).

4.4 Reliability Evaluation by TEG

4.4.1 Test Element Group (TEG)

TEG are test patterns designed to allow evaluation of characteristics and shapes by cutting out and focusing on a certain section when testing with the actual device pattern is difficult.

The Sony Semiconductor Network Company performs evaluation using the dedicated TEG shown in Fig. 4-3 to confirm the basic reliability of structures and materials.

Process evaluation TEG	Pattern shape and machining control TEG	Wire width, film thickness, contact shape, cross-sectional shape, wiring step coverage
	Physical property and basic characteristics evaluation TEG	Endurance voltage, sheet resistance, impurity profile, C-V characteristics, interface state, Vth
	Electrical characteristics evaluation TEG	MOS transistors (Vth, gm), memory cells, BIP transistors, capacitors, polysilicon resistors
Circuit characteristics evaluation TEG	Cell evaluation TEG	I/O cells, ESD protection circuits
	Function block evaluation TEG	DRAM, SRAM, logic circuits, A/D converters
Reliability evaluation TEG	Process TEG	Hot carrier, electromigration, time-dependent dielectric breakdown, plasma damage
	Circuit TEG	DRAM, SRAM and logic circuits
	BIP discrete TEG	Transistors, resistors, capacitors
	Package evaluation TEG	Mechanical stress, aluminum sliding, moisture resistance, soldering heat resistance

Fig. 4-3 TEG Types and Purposes

4.4.2 TEG for Reliability Evaluation

4.4.2.1 Process TEG

Reliability is evaluated in the process development stage using process TEG for each element process to start up and confirm basic reliability.

Evaluation items include gate oxide film reliability, transistor hot carrier degradation, wiring electromigration, stress migration, and so on. These items are evaluated in the assembled package and/or on the wafer.

Table 4-3 Failure Mechanisms and TEG Specifications

Failure mechanism	TEG specifications
Electromigration	Wiring length and width Base grade differences Contact chain
Stress migration	Base grade differences Wiring length
Hot carrier	Transistors (gate length and width) Ring oscillators
Time-dependent dielectric breakdown (TDDB)	MOS capacitors (gate oxide film)

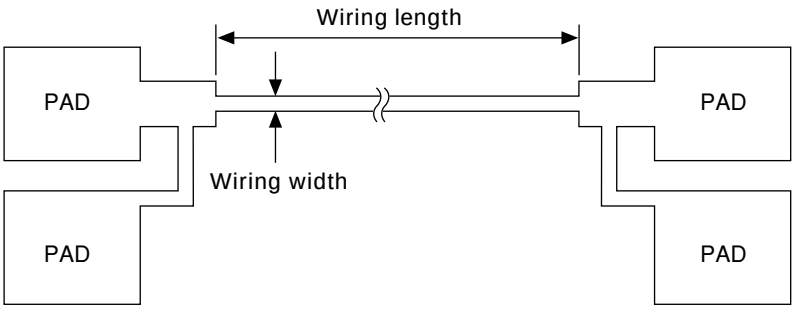


Fig. 4-4 Electromigration Evaluation TEG (Wiring length and width)[1)]

4.4.2.2 Circuit TEG

MOS IC in particular are becoming more complex with increasing circuit scales and mixed mounting of DRAM, and reliability evaluation using actual devices is becoming difficult.

Therefore, during the course of product development, dedicated circuit TEG are created for each logic, DRAM, analog and other circuit, and efficient reliability tests are conducted by dividing devices into elements.

For example, logic circuit reliability is evaluated using SRAM circuit TEG created with the same combination of block elements, and the design is modified to allow easy failure analysis and testing.

4.4.2.3 Bipolar Discrete TEG

When developing a new bipolar process, the reliability of each discrete block element comprising the IC is evaluated. The actual process reliability and problems when integrated into an IC can be understood at an early stage by carrying out this evaluation before IC reliability evaluation.

Discrete TEG include various types of transistors, resistors, capacitors, diodes and so on, and evaluation is possible in a short time by applying high temperature and high humidity bias voltages.

4.4.2.4 Package Evaluation TEG

(1) Development aim

The reliability of mold resin packages has been confirmed to decrease as the mounted chip becomes larger.

The Sony Semiconductor Network Company makes use of this tendency to develop and introduce package evaluation TEG (test element group) chips. These TEG chips allow evaluation with the maximum mountable chip size during new package development, and aim to shorten development and evaluation times and streamline these processes.

(2) TEG specifications

The failure mechanisms that must be confirmed when evaluating package reliability and the corresponding package evaluation TEG specifications are summarized in Table 4-4. In addition, Fig. 4-5 shows an actual layout image.

These TEG allow basic evaluation of package cracking, assembly performance, and the effects of various package-induced damage on chips.

Table 4-4 Failure Mechanisms and TEG Specifications

Failure mechanism		TEG specifications
Package cracking	Resin cracking, gold wire open connections and package expansion caused by the package size and mold resin moisture absorption characteristics	Evaluate at different sizes according to the chip size and package.
Passivation film cracking	Metallic wiring corrosion and migration caused by filler attack, scratches and rubbing	Position wide aluminum wiring in the center of the chip, and check for electrical open or short defects between metallic wiring caused by damage to the passivation or interlayer films.
Aluminum sliding	Metallic wiring open connections and migration caused by mold resin stress	Position aluminum wiring in the chip corners which are susceptible to resin stress, and check for electrical open or short defects between metallic wiring.
Moisture penetration between layers	Wiring open connections, corrosion and ion contamination caused by the penetration of water between the passivation film and metallic wiring or between metallic wiring layers	Position aluminum wiring at the chip edges which are susceptible to moisture penetration and check for electrical open or short defects between metallic wiring.
Chip cracking	Short circuit and leakage defects caused by chip cracking	
Aluminum corrosion	Aluminum wiring corrosion caused by the penetration of water between the passivation film and metallic wiring or between metallic wiring layers	Remove the passivation film from a certain area and check for electrical open defects in the outermost layer of wiring in this area.
Assembly fluctuation	IC characteristics fluctuation before and after encapsulation in mold resin	Position polysilicon resistors in the chip corners which are susceptible to plastic stress, and check the resistance value fluctuation. Also check the transistor operation.
Bonding defects	Wire bonding conditions Cratering, purple plague and bonding peeling caused by the structure under the pad	Evaluate each of these items individually in the die bonding and wire bonding processes.

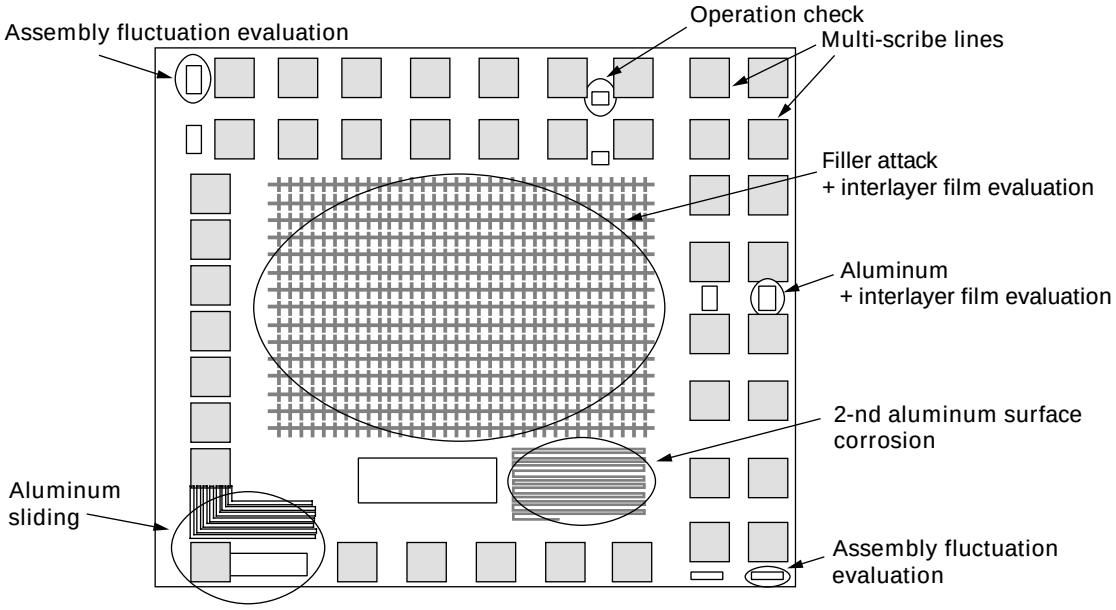
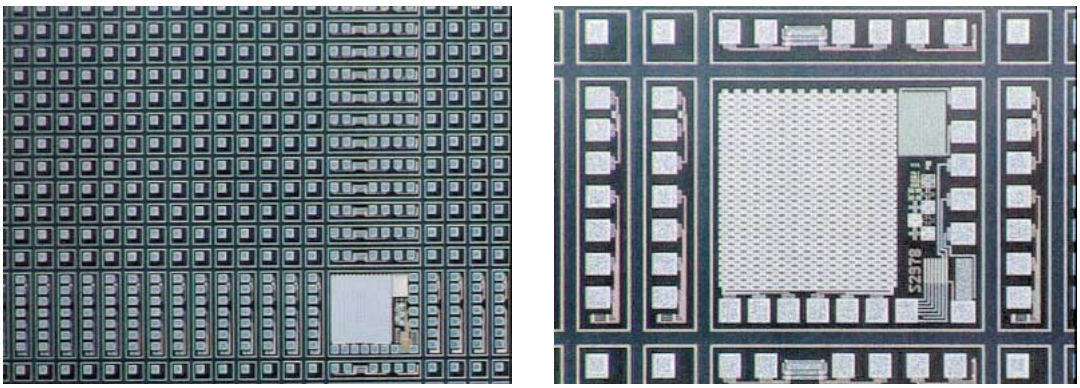


Fig. 4-5 Layout Image

(3) TEG

Photos 4-1(a) and (b) show enlarged photos of a TEG.

This chip employs multi-scribe lines, and the size can be changed in 0.3 mm increments.



(a) Entire chip (b) TEG circuit block

Photo 4-1 Package Evaluation TEG

4.4.3 Reliability Evaluation Methods Using TEG

When evaluating the reliability of semiconductor devices, it is extremely difficult to narrow down reliability problems, particularly those rooted in processes, by evaluating complex integrated circuits such as products. Therefore, detecting reliability problems which may occur at the product stage as early as possible and providing feedback to design and the processes is absolutely essential for establishing high reliability processes and ensuring high product reliability.

Various methods are employed using TEG to quickly clarify failure mechanisms, calculate life prediction parameters, and evaluate mass production process stability, etc.

4.4.3.1 Wafer Level Reliability (WLR)

This method allows easy and speedy evaluation of process reliability at the wafer level for reliability tests using products assembled into packages and TEG.

(1) Features:

TEG are created beforehand for each conceivable failure mechanism, and evaluated using a dedicated measurement program. The advantages of this method are as follows.

- Large amounts of data can be acquired in a short time with the dedicated measuring system.
- The evaluation time can be shortened by carrying out high acceleration tests.
- The reliability of element processes can be evaluated without time-consuming failure analysis.

(2) Applications:

① **Process development stage**

Possible applications as tools supporting the quick start-up of high reliability processes are as follows.

(Examples)

- Evaluation of process reliability before product and TEG reliability tests
- Evaluation of reliability stability and variance during the course of process development
- Relative evaluation and confirmation evaluation when selecting processes, etc.

② **Production stage**

Possible applications as tools for monitoring reliability in the production process are as follows.

(Examples)

- Preemptive detection of reliability problems
- Monitoring of process reliability stability at the production stage
- Go/No Go evaluation of production process changes, etc.

(3) TEG types:

Typical WLR TEG types are as follows.
DRAM cell capacitor film reliability evaluation TEG
Gate oxide film reliability evaluation TEG
Electromigration evaluation TEG
Stress migration evaluation TEG
Hot carrier degradation evaluation TEG
Process charge damage evaluation TEG, etc.

<References>

1) "Standard Guide for Design of Flat, Straight-Line Test Structures for Detecting Metallization Open-Circuit or Resistance-Increase Failure Due to Electromigration", Annual Book of ASTM Standards, Vol.10.04 F1259 (1989).

4.5 Reliability Prediction

4.5.1 Semiconductor Device Failure Rate

In general, the semiconductor device failure rate distribution over time is governed mainly by the initial failure and wear-out failure rates as mentioned in section 4.1. This section provides a detailed description of the Sony Semiconductor Network Company's approach toward semiconductor device failure rates.

4.5.1.1 Semiconductor Device Failure Regions

Fig. 4-6 shows the time-dependent change in the semiconductor device failure rate. Like general electronic equipment, discussions on semiconductor device failure regions often classify failure regions into the three types of initial, random and wear-out failure regions. However, there is no clear definition for determining the boundary between these regions. When drawing time-dependent failure rate curves, the sum of the initial, random and wear-out failure rates can be thought to indicate the transition in the semiconductor device failure rate as shown in Fig. 4-6.

The reliability index used when discussing semiconductor device failure rates thus far has been the average failure rate (FIT value (10^{-9}/device hours)) which follows an exponential distribution with the constant failure rate generally used for system reliability. However, semiconductor devices are manufactured by highly controlled processes, and the failure modes and degradation mechanisms have been clarified to a certain degree. Therefore, viewed in terms of failure mechanisms, randomly occurring failures which are thought to be due to failure modes are virtually nonexistent. Based on the symptoms and results of failure analysis, most failures occurring in reliability tests or in the market can be presumed to be initial failures caused by initial defects or wear-out failures. Therefore, the initial and wear-out failure rates are thought to be important indices in current failure rate prediction for semiconductor devices.

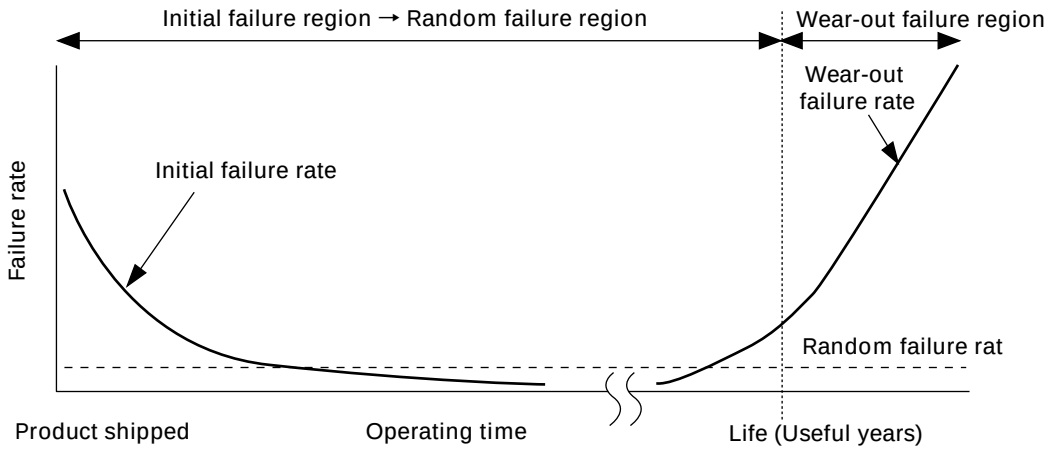


Fig. 4-6 Time-Dependent Change in Semiconductor Device Failure Rate

4.5.1.2 Initial Failures

The failure rate in the initial failure period is called the early failure rate (EFR), and exhibits a shape where the failure rate decreases over time. The vast majority of semiconductor device initial defects are caused by defects built into devices mainly in the wafer process. The most common causes of these defects are dust adhering to wafers in the wafer process and crystal defects in the gate oxide film or the silicon substrate, etc.

Most devices containing defects rooted in the manufacturing process fail within the manufacturing process and are eliminated as defective in the final sorting process. However, a certain percentage of devices with relatively insignificant defects may not have failed when making the final measurements and may be shipped as passing products. These types of devices which are inherently defective from the start often fail when stress (voltage, temperature, etc.) is applied for a relatively short period, and exhibit a high failure rate in a short time within the customer's mounting process or in the initial stages after being shipped as products. However, these inherently defective devices fail and are eliminated over time, so the rate at which initial failures occur decreases.

Eventually, when most of these defective devices have failed and been eliminated, the initial failure rate drops to a level which can be ignored. The failure rate at this stage decreases gradually as an extension of the initial failure rate, but since there are almost no failures, the failure distribution takes the appearance of a random failure region where failure rate does not change.

This property of semiconductor devices where the failure rate decreases over time can be used to perform screening known as "burn-in" where stress is applied for a short time in the stage before shipping to eliminate devices containing initial defects. Product groups from which devices with inherent initial defects have been removed to a certain degree by burn-in not only improve the initial failure rate in the market, but also make it possible to maintain high quality over a long period as long as these products do not enter the wear-out failure region.

(1) Methods for estimating the initial failure rate

Time-dependent changes in the initial failure rate can be estimated by processing failure data obtained by the burn-in study method using a Weibull probability distribution. Burn-in study refers to the method where burn-in is performed consecutively multiple times in a short period under highly accelerated conditions using a sample quantity on a scale which is certain to contain devices with inherent initial devices (normally several thousand to ten thousand pieces). After that the failure data for each measurement time is used to obtain the time-dependent changes in the initial failure rate.

When multiple initial failure rate data obtained through the burn-in study are applied to the following Weibull distribution failure distribution function,

$$F(t) = 1 - \exp\left\{-\left(\frac{t}{\eta}\right)^{m}\right\}$$

the values of shape parameters m and $\ln(t_0)$ can be obtained from the regression line derived from the multiple data as shown in Fig. 4-7. (See Appendix 4-3.)

Furthermore, the cumulative initial failure rate up to the desired time in the market environment can be obtained from the burn-in study conditions and the market environment conditions. (Fig. 4-8)

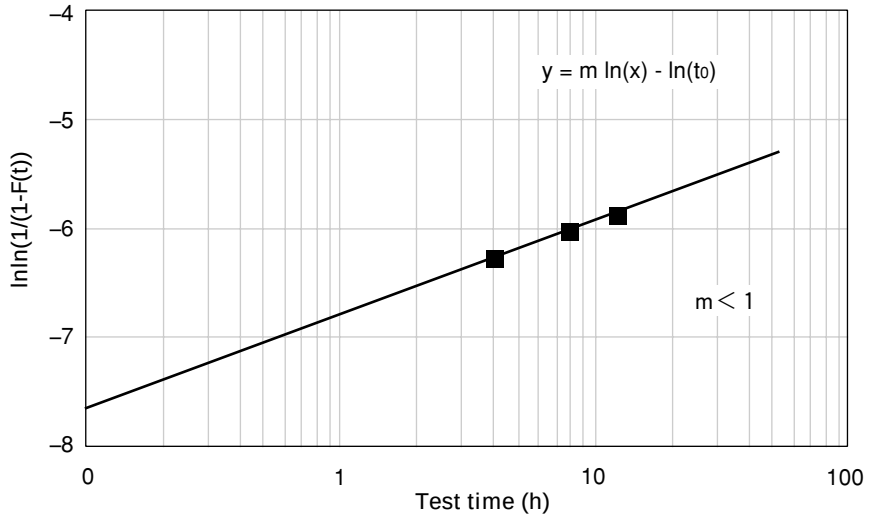


Fig. 4-7 Regression Line Obtained from the Weibull Plot of the Burn-in Study Results

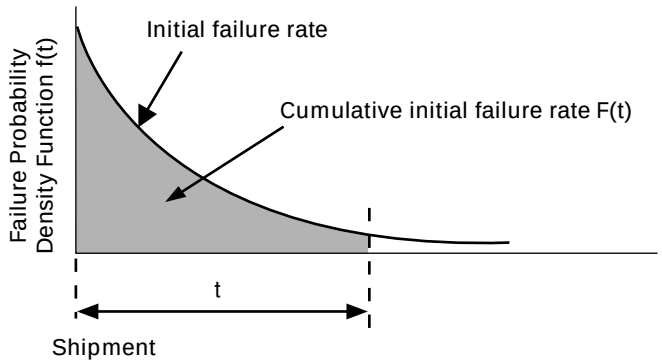


Fig. 4-8 Initial Failure Rate Curve and Cumulative Failure Rate up to Time t

(2) Determining the burn-in conditions

The screening (burn-in) conditions required to reduce the initial failure rate after shipment to the target value can be determined using the failure distribution function F(t) obtained from the burn-in study.

Labeling the burn-in time as t_0 and the coefficient of acceleration for the burn-in conditions and the market environment as K, the cumulative initial failure rate that can be eliminated by burn-in is given as $F(K \cdot t_0)$, and the new cumulative initial failure rate F(t) up to time t after burn-in can be obtained by the following formula.

$$F(t) = F(K \cdot t_0 + t) - F(K \cdot t_0)$$

This relationship can be expressed in graph form as shown in Fig. 4-9.

The burn-in conditions are selected according to the combination of the acceleration conditions and time that will reduce this value to the target initial failure rate or lower.

Normally, initial defects which are the cause of initial failures occur at the highest rate in the initial stages of process development, and then decrease thereafter due to process improvements and process mastery. The initial failure rate decreases in proportion to these initial defects, so the burn-in time is reviewed as appropriate in accordance with process improvements.

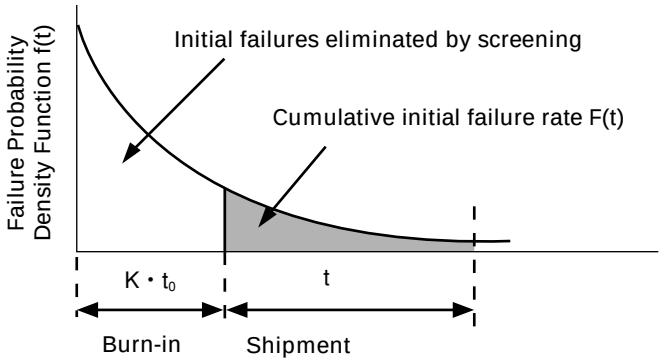


Fig. 4-9 Initial Failure Screening by Burn-in

4.5.1.3 Random Failures

When devices containing initial defects have been eliminated to a certain degree, the initial failure rate becomes extremely small, and the failure rate exhibits a gradually declining curve over time. In this state, the failure distribution is close to an exponential distribution, and this is called the random failure period. The semiconductor device failure rate during this period is an extremely small value compared to the initial failure rate immediately after shipment, and is normally a level which can be ignored for the most part. Viewed in terms of failure mechanisms, there are extremely few semiconductor device failures that can be clearly defined as random failures. However, memory software errors and other phenomena caused by α rays and other high energy particles are sometimes classified as randomly occurring failure mechanisms.

When predicting semiconductor device failure rates, failures occurring sporadically after a certain long time has passed since the start of operation and failures for which the failure cause could not be determined are treated as random failures in some cases. However, most of these failures are thought to be devices containing relatively insignificant initial defects (dust or crystal defects) which fail after a long time, and should essentially be positioned on the initial failure rate attenuation curve. This type of failure rate cannot be estimated from the results of tests performed with few samples such as reliability tests.

There are also phenomena such as ESD breakdown, overvoltage (surge) breakdown (EOS) and latch-up which occur at random according to the conditions of use. However, these phenomena are all produced by the application of excessive stress over the device absolute maximum ratings, so these are classified as breakdowns instead of failures, and are not included in the random failure rate.

4.5.1.4 Wear-out Failures

Wear-out failures are failures rooted in the durability of the materials comprising semiconductor devices and the transistors, wiring, oxide films and other elements, and are an index for determining the device life (useful years). In the wear-out failure region, the failure rate increases with time until ultimately all devices fail or suffer characteristic defects. (Fig. 4-10)

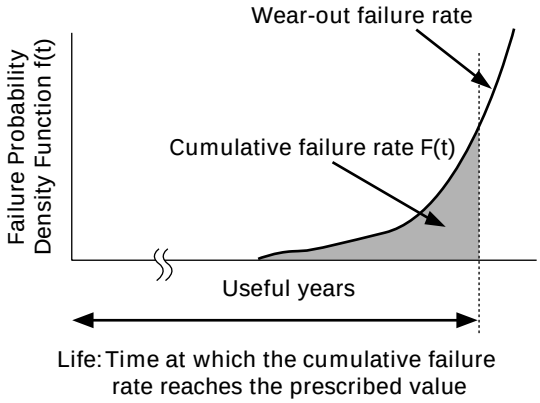


Fig. 4-10 Wear-out Failure Rate Curve and Life

The main wear-out failure mechanisms for semiconductor devices are as follows.

- Electromigration
- Hot carrier-induced characteristics fluctuation
- Time-dependent dielectric breakdown (TDDB)
- Laser diode luminance degradation

Semiconductor device life is defined as the time (or stress) at which the cumulative failure rate for the wear-out failure mode reaches the prescribed value, and can be estimated using the results of reliability tests and test element group (TEG) evaluation. Semiconductor device life is often determined by the reliability of each element (wiring, oxide film, interlayer film, transistor) comprising the device, and these reliabilities are evaluated using discrete element TEG in the process development stage. These TEG evaluation results are incorporated into design rules in the form of allowable stress limits (electric field strength, current density, etc.) to suppress wear-out failures in the product stage and ensure long-term reliability. As a result, semiconductor devices experience almost no wear-out failures within the reliability test time (stress) range in the product stage.

(1) Life estimation method

Semiconductor device life can be obtained as follows based on the wear-out failure data generated by TEG evaluation and reliability tests. First linear regression is performed for the time-dependent cumulative failure rate using a Weibull probability distribution or logarithmic normal probability distribution, then the life is obtained from the time (or stress) at which the reference cumulative failure rate is reached and the acceleration multiple of the accelerated test conditions (Fig. 4-11).

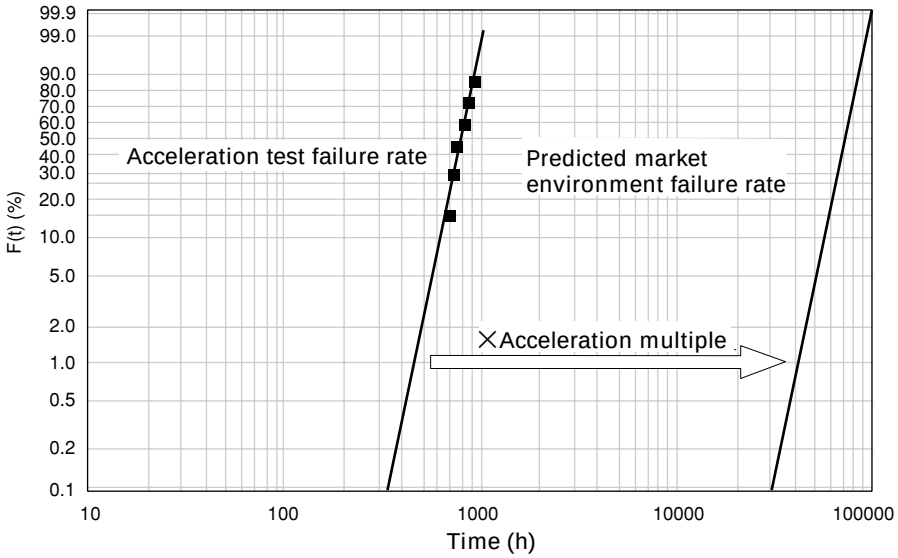


Fig. 4-11 Failure Rate Prediction Method Using Weibull Probability Plotting Paper

4.5.2 Acceleration Theory

Semiconductors experience characteristics degradation and failure due to temperature, humidity and other external environmental conditions and stress such as heat generation, voltages and currents during operation, etc. This section derives acceleration factors from the basic formulas stating how life is affected by the size of each stress. Acceleration factors represent the ratio of the life in the customer's operating stress environment to the life in the reliability test, burn-in or other stress environment. For example, if the life in the customer's operating stress environment is 10 years and the life in the reliability test stress environment is 0.1 year, the acceleration factor is 10 years/0.1 years = 100 times.

(1) Temperature acceleration

Generally, most failure mechanisms are promoted by exposure to high temperatures. The life temperature acceleration factor K at this time can be obtained from the Arrhenius model using the following formula.

$$K \equiv \frac{\tau_F}{\tau_E} = \exp\left\{\frac{Ea}{k}\left(\frac{1}{T_F} - \frac{1}{T_E}\right)\right\}$$

Where,

τ_F : Market life
τ_E : Reliability test life
T_F : Market operating temperature
T_E : Test temperature

(2) Acceleration factors other than temperature

The actual semiconductor life also changes according to stress factors other than temperature such as temperature and humidity, temperature and voltage, and temperature and current. These cases use the following life formula which adds another stress item to the above mentioned temperature item.

$$\tau = A\exp(-\beta \cdot S)\cdot\exp\left(\frac{Ea}{kT}\right)$$

Where,
β : Constant
S : Non-temperature stress

Note that the following formulas may be used, but these formulas are mathematically equivalent.

When $\gamma \equiv \beta/\ln(10)$

$$\tau \propto 10^{-\gamma S}\cdot\exp\left(\frac{Ea}{kT}\right)$$

When $S' \equiv \exp(S)$

$$\tau \propto S'^{-\beta}\cdot\exp\left(\frac{Ea}{kT}\right)$$

Like the Arrhenius model, labeling the operating or storage stress as S_F, the reliability test stress as S_E, and the respective lives as τ_F and τ_E, the acceleration factor K is given by the following formula.

$$\begin{aligned} K &\equiv \frac{\tau_F}{\tau_E} \\ &= \exp\{-\beta(S_E - S_F)\}\cdot\exp\left\{\frac{Ea}{k}\left(\frac{1}{T_F}-\frac{1}{T_E}\right)\right\} \\ &= 10^{-\gamma(S_E-S_F)}\cdot\exp\left\{\frac{Ea}{k}\left(\frac{1}{T_F}-\frac{1}{T_E}\right)\right\} \\ &= \left(\frac{S'_E}{S'_F}\right)^{-\beta}\cdot\exp\left\{\frac{Ea}{k}\left(\frac{1}{T_F}-\frac{1}{T_E}\right)\right\} \end{aligned}$$

Assuming $\beta_1 = \beta$, $S_1 = S$, $\beta_2 = \frac{Ea}{k}$, $S_2 = \frac{1}{T}$ the life formula can be transformed into a formula for general stress as follows.

$$\tau = A\exp(-\beta_1 \cdot S_1)\cdot\exp(-\beta_2 \cdot S_2)$$

When there are n stress factors, an even more general formula is obtained.

$$\tau = A\exp(-\beta_1 \cdot S_1)\cdot\exp(-\beta_2 \cdot S_2)\cdot\cdots\cdot\exp(-\beta_n \cdot S_n)$$

Labeling the operating or storage stress as S_{iF} (i = 1,..., n), the reliability test stress as S_{iE} (i = 1,..., n), and the respective lives as τ_F and τ_E, the acceleration factor is given by the following formula.

$$K \equiv \frac{\tau_F}{\tau_E} = \exp\{-\beta_1(S_{1E}-S_{1F})\}\cdot\cdots\cdot\exp\{-\beta_n(S_{nE}-S_{nF})\}$$

4.5.3 Stress Acceleration Tests

In order to obtain acceleration factors, tests are carried out by varying stress and the acceleration factors are calculated based on these results.

Voltage acceleration is used here as an example.

Voltage acceleration is given by substituting n = 1 and voltage S = V to the general life formula.

$$\tau = A\exp(-V \cdot \beta)$$

If the constants A and β are known, the relationship between the voltage V and life τ can be clarified. Therefore, these constants can be calculated by experimentally obtaining the life at multiple voltages.

Taking the natural logarithm ln, the above formula can be transformed as follows.

$$\ln\tau = \ln A - \beta \cdot V$$

β can be obtained from the slope when plotting this formula with the voltage V as the horizontal axis and the life τ as the vertical axis. (Fig. 4-12)

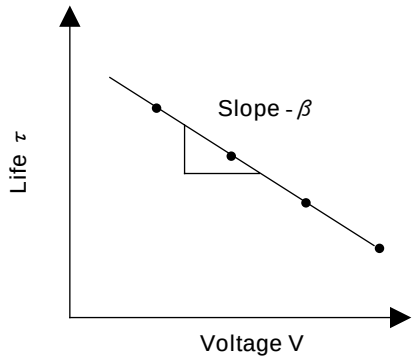


Fig. 4-12 Relationship between Voltage and Life τ

The life also contains variance which is not due to stress. This variance follows a Weibull or logarithmic normal distribution, but in consideration of the distribution with respect to individual stresses, η and μ are used in place of τ for the Weibull and logarithmic normal plots, respectively.

A typical stress acceleration test procedure is described below.

(1) Perform the stress acceleration test.

(2) Obtain the cumulative failure rate.

(3) Draw the Weibull or logarithmic normal plots. Fig. 4-13 shows the plots for the four voltage conditions of V_1, V_2, V_3 and V_4.

(4) Read η or μ from the plots.

(5) Plot the relationship between the stress and η or μ.

(6) Read the constant from the plotted slope.
In this voltage acceleration example, read β from the graph. (Fig. 4-14)

(7) Obtain the acceleration factor.
For example, the acceleration factor between the test voltage and the market voltage is as follows.

$$K = \exp\{-\beta(V_E - V_F)\}$$

Where,
V_E: Test voltage V_F: Market operating voltage

(8) The acceleration factor is useful for determining the burn-in time or estimating the life.

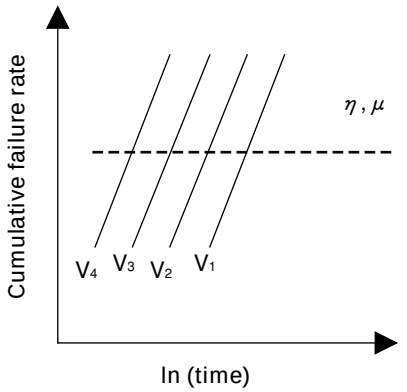


Fig. 4-13 Weibull Plots for Different Voltage Conditions

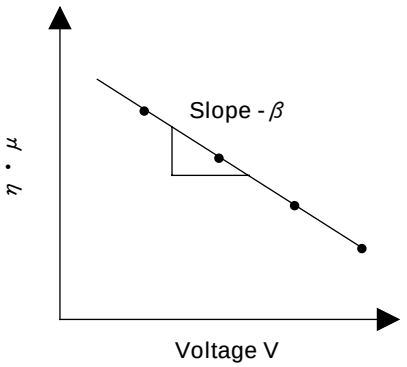


Fig. 4-14 Relationship between Voltage and Life $\eta \cdot \mu$

4.5.4 Failure Rate Prediction Case Studies

(1) Estimation of hot carrier degradation life for a high speed CMOS logic IC

Subject: C6 series (0.25 μm) logic IC with a system clock of approximately 600 MHz
Failure mechanism: Drain avalanche hot carrier (DAHC)

$$\tau \propto V^{-n} \cdot \exp\left(\frac{Ea}{kT}\right)$$

Where,
V : Supply voltage T : Temperature

Acceleration factor $$K = \left(\frac{V_E}{V_F}\right)^n \cdot \exp\left\{\frac{Ea}{k}\left(\frac{1}{T_F} - \frac{1}{T_E}\right)\right\}$$

Where,
T_E : Test temperature T_F : Market operating temperature

Reliability test: Low temperature operation and high temperature operation tests with the system clock held constant at approximately 600 MHz regardless of the supply voltage and temperature

Fig. 4-15 shows the reliability test results.

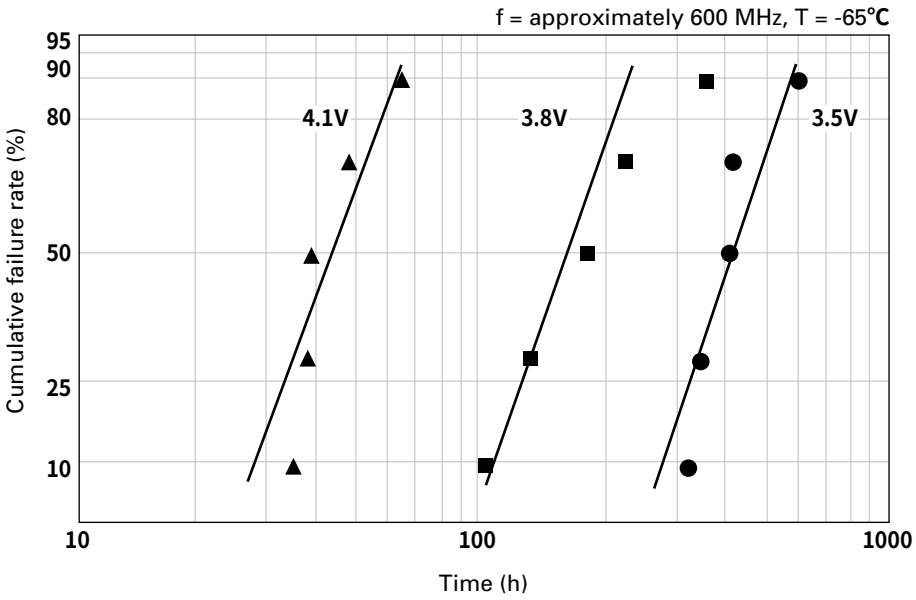


Fig. 4-15 Logarithmic Normal Plot of Hot Carrier Failure

Logarithmically plotting both the average failure rate μ and the voltage V from this logarithmic normal plot yields the results shown in Fig. 4-16. The constant n which represents the voltage acceleration characteristics can be obtained from this slope.

n = 14.1

Regarding temperature acceleration, the activation energy Ea = -0.049 [eV] was obtained from the test results at T = -65°C to +125°C. At this point, the test acceleration characteristics are obtained as follows using the voltage acceleration factor for an actual IC operating voltage V_F = 2.5 V and reliability test condition V_E = 3.5 V, and the temperature acceleration factor for an actual IC operating temperature T_F = 55°C and reliability test condition T_E = -65°C.

$$K=\left(\frac{V_E}{V_F}\right)^{14.1}\cdot\exp\left\{\frac{-0.049}{k}\left(\frac{1}{T_F}-\frac{1}{T_E}\right)\right\}$$

$$= 312 \text{ times}$$

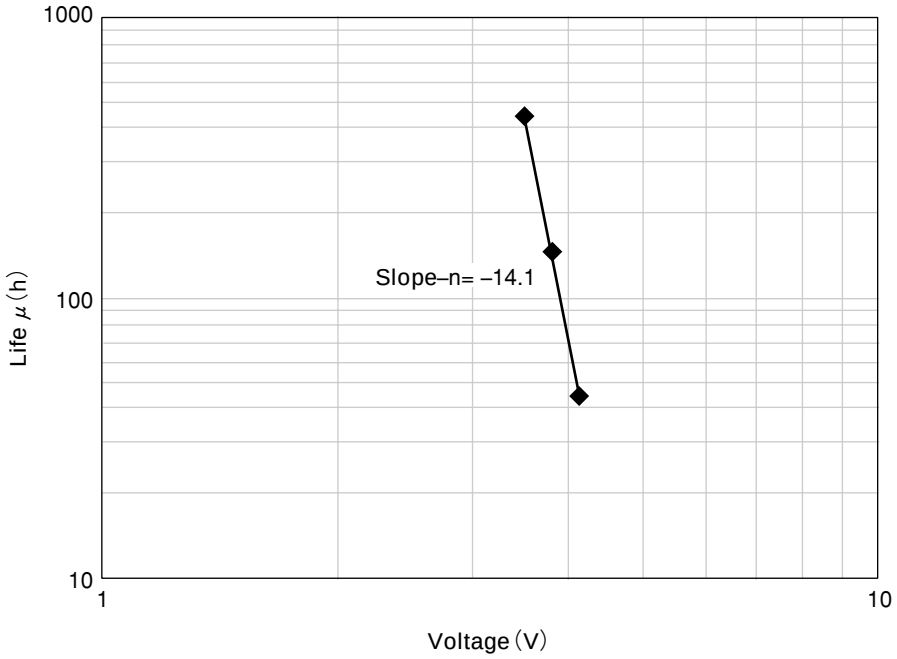


Fig. 4-16 Hot Carrier Voltage Acceleration Characteristics

The failure rate graph under actual operating conditions can be obtained by multiplying the average life μ obtained from the logarithmic normal plot of the test results at T = -65℃ and V = 3.5 V with the acceleration factor K = 423 times, and drawing a straight line with the same slope through this value. (Fig. 4-17) The life t_{50} at which half of these devices will fail can be estimated from this graph as 1.8×10^5 [h] = 20.5 years.

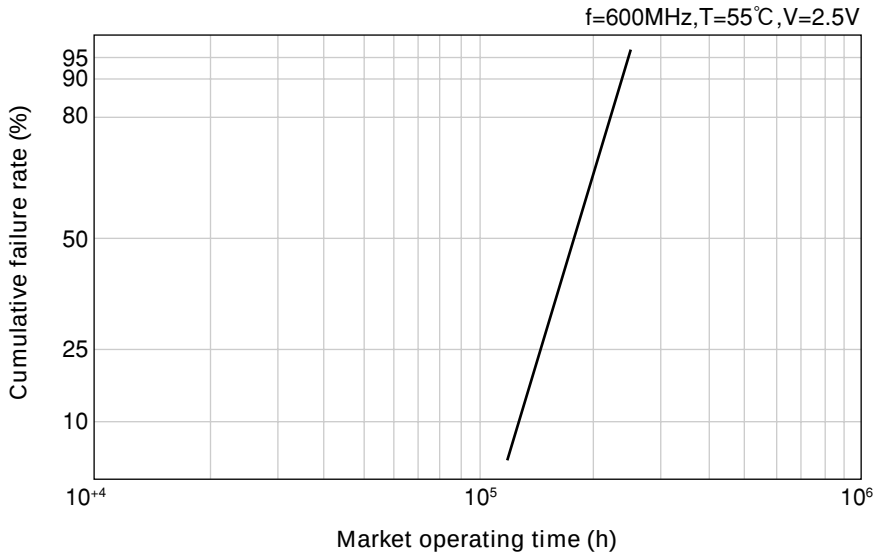


Fig. 4-17 Logarithmic Normal Plot of Hot Carrier Failure

(2) Estimation of BGA thermal stress reliability life

Subject : BGA package for system LSI

Failure mechanism : BGA wiring substrate open connection failure caused by cracking when thermal stress is applied to the semiconductor mold resin

$$\tau \propto f^{m}(\Delta T)^{-n}\exp\left(\frac{Ea}{kT_{max}}\right)$$

Where,

ΔT : Temperature difference

n, m : Constants

Assuming the stress to be dependent only on the temperature difference ΔT,

$$\tau \propto (\Delta T)^{-n}$$

Accordingly, the acceleration factor K is:

$$K=\left(\frac{\Delta T_E}{\Delta T_F}\right)^{n}$$

Where

ΔT_E : Test temperature difference ΔT_F : Market temperature difference

Reliability test : Temperature cycle test with varying temperature differences ΔT

Fig. 4-18 shows the reliability test results.

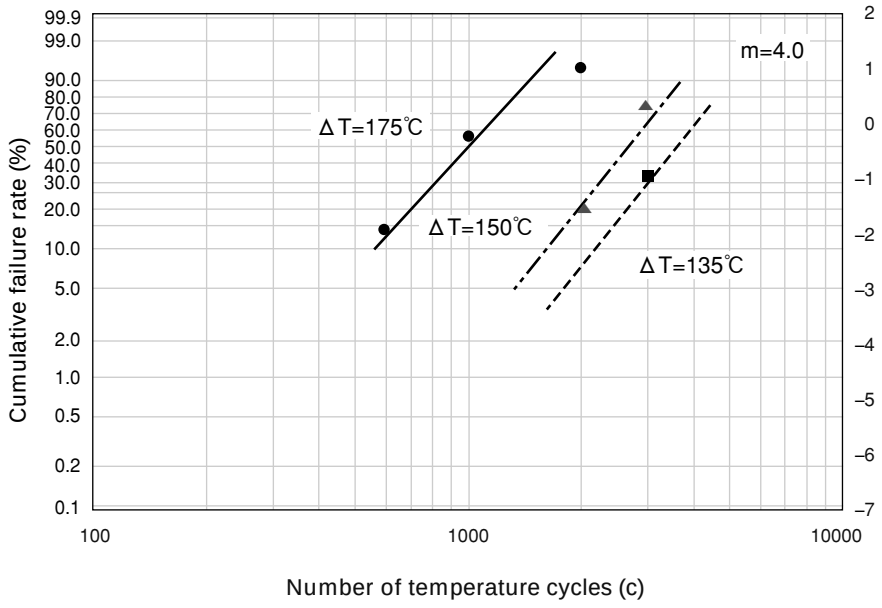


Fig. 4-18 BGA Package Temperature Cycle Test Results[1)]

Logarithmically plotting both the life η and the temperature difference ΔT from this Weibull plot yields the results shown in Fig. 4-19. The constant n which represents the temperature acceleration characteristics can be obtained from this slope.

n = 4.9

The acceleration factor for market condition $\Delta T_F = 50℃$ and test condition $\Delta T_E = 150℃$ is as follows.

$$K = \left(\frac{\Delta T_E}{\Delta T_F}\right)^{4.9}$$

$$= 217 \text{ times}$$

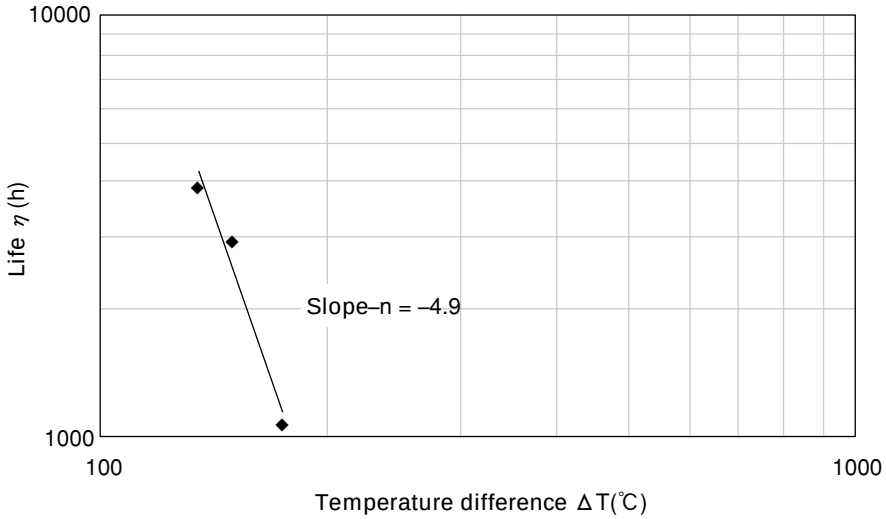


Fig. 4-19 Cracking Dependency on Temperature Difference

In addition, the actual operating environment life t_{50} is given as follows by multiplying the t_{50} value obtained from the test results at $\Delta T = 150℃$ by the acceleration factor K.

$$t_{50} = 2700 \text{ cycles} \times 217 \text{ times} = 5.9 \times 10^5 \text{ cycles}$$

These results correspond to a life of approximately 1,000 years or more assuming the usage where the product is turned on and off one time per day.

(3) Estimation of DRAM fuse moisture resistance life

Subject : 0.35 µm generation DRAM

Failure mechanism : Memory device fuse circuit element corrosion

$$\tau \propto P_{H_2O}^{-n}$$

Where,
P_{H_2O} : Steam pressure

Acceleration factor $K = \left(\frac{P_E}{P_F}\right)^n$

Where,
P_E : Test steam pressure
P_F : Market storage environment steam pressure

Reliability test : Pressure cooker test using three different steam pressures

Fig. 4-20 shows the reliability test results.

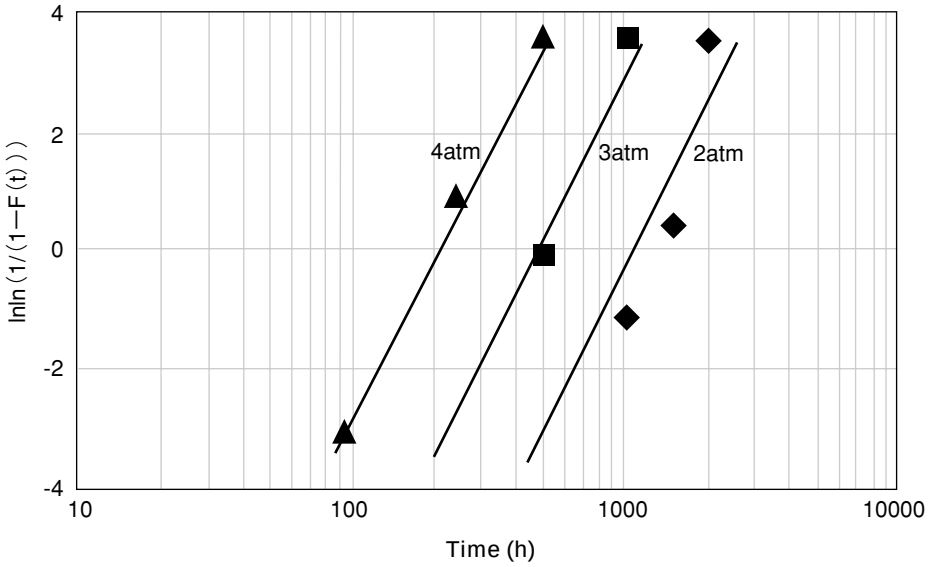


Fig. 4-20 Weibull Plot for Fuse Corrosion Failure

Reading the parameter η from the Weibull plot in Fig. 4-20, the steam pressure acceleration characteristics constant n can be obtained from the relationship between the average life η and the steam pressure shown in Fig. 4-21.

n = 2.82

When the actual operating environment conditions are 30℃ and 85% RH, the steam pressure is $P_F = 3.606 \times 10^3$ Pa, so the acceleration factor at the test condition $P_E = 2.03 \times 10^5$ Pa is given as follows.

$$K = \left(\frac{P_E}{P_F}\right)^{2.82}$$

$$= 8.74 \times 10^4 \text{ times}$$

In addition, the life t_{50} in the actual operating environment is given as follows by multiplying the t_{50} value obtained from the test results at PE = 2.03×10^5 Pa by the acceleration factor K.

$$t_{50} = 1.23 \times 10^3 \times 8.74 \times 10^4 = 1.08 \times 10^8 \text{ hours} = 12{,}300 \text{ years}$$

These results show that the life is semi-permanent even for storage at the high temperature and high humidity of 30℃ and 85% RH.

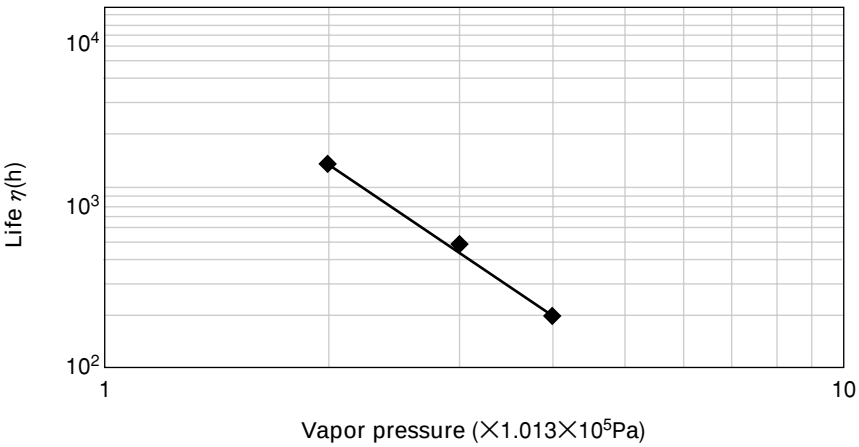


Fig. 4-21 Vapor Pressure Acceleration Characteristics

<References>

1) Shiraishi et al., “Investigation of a Life Model in Temperature Cycle Evaluation of BGA Packages”, Preliminary Manuscripts for the 9th RCJ Reliability Symposium, pp.43, (1999).

4.6 Test Coverage

Test coverage generally refers to the random gate test quality, and is defined as follows.

Test coverage [%] = 100 × Number of detected failures/Total number of failures

The number of failures here is normally the number of failures hypothesized by the simple degenerative failure model. The degenerative failure model is a failure model which simplifies various real failures into the two types of short circuits with GND (0 degenerative failures) and short circuits with V_{DD} (1 degenerative failures). The simple degenerative failure model is a further simplified model which assumes that these degenerative failures exist at only one location within a circuit. This simple degenerative failure model is used for failure simulations and automatic test pattern generation (ATPG) using scan path test facilitating designs. These simple degenerative failures assume that there are two 0 degenerative failures and two 1 degenerative failures in each of the input/output pins of all gates. This total number is used as the total number of failures, and of these the tested failures are used as the number of detected failures.

A different type of test coverage can be considered for memory cells and analog elements, etc.

In contrast to random gates, memory cells have a regular and highly integrated structure, and are designed using transistors and wiring. Therefore, test patterns which hypothesize more specific failures and have a test coverage of 100% are designed and used. Well-known test patterns of this type include matching patterns and checkerboard patterns.

When LSI manufacturers create test patterns using memory test facilitating designs (direct access from the chip pins, build-in self test (BIST), etc.), the test coverage need not be taken into account.

There is also no concept of test coverage for analog elements. This is because analog elements generally have irregular structures and are designed using various transistors and wiring, which makes simplifying potential failures or focusing on particular failures difficult. Therefore, analog elements are tested based on their individual specifications.

In addition to test coverage, the process yield is also related to LSI quality. Even with the same test coverage, higher quality can generally be obtained by manufacturing with a high yield process than a low yield process. Stated another way, when using the latest processes, test facilitating designs (scan path, memory build-in self test, etc.) should be actively applied to increase the test coverage as much as possible.

4.7 Reliability Related Standards

There are numerous standards related to semiconductor device reliability, and these standards can be broadly classified as shown in Table 4-5. Among these standards, activities have increased recently toward the adoption of international standards from the viewpoint of eliminating import-export barriers and technical obstacles for international trade. The Sony Semiconductor Network Company is an active participant in various standardization committees both domestically and in the U.S. and Europe, and promotes vigorous standardization activities.

Table 4-5 Reliability Related Standards

International standards	ISO, IEC
Regional standards	CEN, CENELEC (Europe)
National standards	JIS (Japan), ANSI (U.S.), BS (England),・・・
Public agency standards	MIL (U.S. Department of Defense),・・・
Industry standards, etc.	EIAJ, JASO, RCJ, EIA/JEDEC, UL, ・・・

ISO: International Standard Organization
IEC: International Electrotechnical Commission
JIS: Japanese Industrial Standard
BS: British Standard
MIL: Military Standard
EIAJ: Electronic Industries Association of Japan
RCJ: Reliability Center for Components of Japan
JEDEC: Joint Electron Device Engineering Council
EIA: Electronic Industries Association
UL: Underwriters Laboratories
ANSI: American National Standards Institute
CEN: Comite Européen de Normalisation
CENELEC: Comite Européen de Normalisation Électrotechnique
JASO: Japanese Automobile Standards Organization

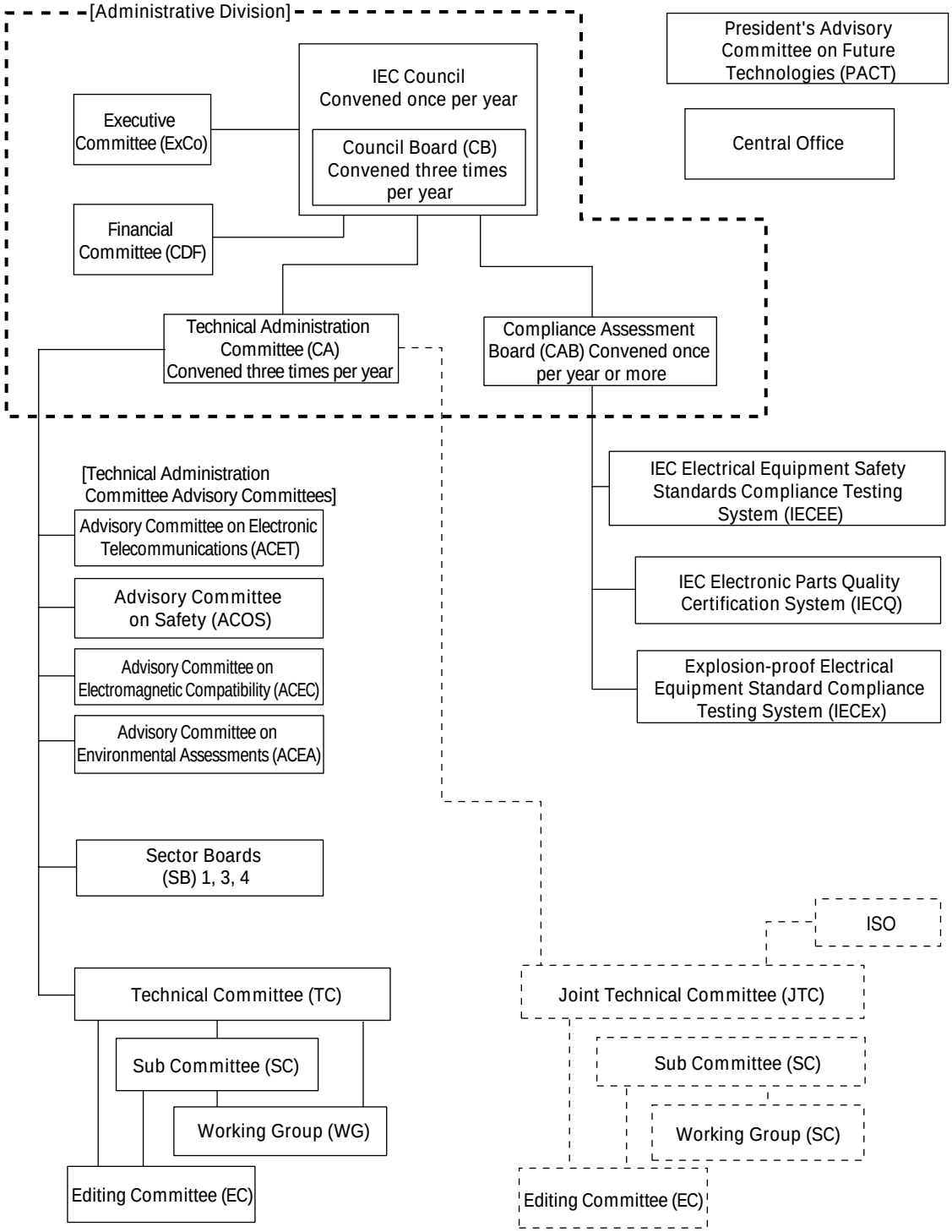
(1) IEC (International Electrotechnical Commission)

IEC was founded in 1908 as a private nonprofit foundation based on the Swiss Civil Code. However, it has currently reached a status where it is treated roughly on a par with the United Nations as an international standards organization, and is acknowledged as a world standard even in the Agreements of the World Trade Organization (WTO) technological Barrier for Trade (TBT).

IEC's stated purpose is to "promote international cooperation related to standardization in the electric and electronic technology fields, and to work toward a mutual international understanding." IEC establishes standards for terminology, symbols, ratings, various test methods and other items for all electric and electronic fields except information technology.

IEC has established technical committees (TC) and affiliated sub committees (SC) for each technical field, and institutes standards based on an “international consensus” after years of phased deliberations. The IEC organization diagram is shown in Table 4-6.

Table 4-6 IEC (International Electrotechnical Commission) Organization Diagram



Note that only one representative organization per country is qualified for IEC membership. In Japan this is the Japan Industrial Standards Committee (JISC) established under the Industrial Standards Act. The Standards Department of the Agency of Industrial Science and Technology, Ministry of International Trade and Industry serves as the JISC Secretariat.

Examples of IEC standards related to reliability are shown in Table 4-7 below.

Table 4-7 IEC Standards

IEC60695	Fire resistance testing methods for general parts
IEC60068	Environmental testing methods for general parts
IEC60747	Specifications by semiconductor device type
IEC60748	Specifications by semiconductor integrated circuit type
IEC60749	Mechanical and weather resistance testing methods for semiconductor devices

(2) EIAJ (Electronic Industries Association of Japan)

EIAJ is an industry body established in 1948 which deliberates and establishes standards to promote smooth business transactions in the fields of consumer and industrial use electronic equipment, electronic parts and devices. Together with the Japan Electronic Industry Development Association (JEIDA) and Japan Electrical Manufacturers' Association (JEMA), EIAJ activities fulfill essential standardization functions domestically within Japan. In addition, EIAJ promotes activities to advocate EIAJ standards (drafts) as IEC standard proposals, and functions as a liaison with EIA, JEDEC and other related overseas committees. The Sony Semiconductor Network Company is an active participant in various EIAJ committees, and deploys standardization activities.

JIS standards (JIS C 7021, 7022) concerning semiconductor device reliability were abolished in 1997, and currently EIAJ is the Japanese domestic standard which is most often used as a reference for determining actual test methods, etc. These contents are also extremely practical, and could be called advanced. Table 4-8 shows the EIAJ standards concerning semiconductor reliability.

Table 4-8 EIAJ Standard Types

ED-4701（1992）	Environmental and durability testing methods for semiconductor devices
ED-4701-1（1994）	Environmental and durability testing methods for semiconductor devices Supplement 1) ESD breakdown test (Human Body Model), etc.
ED-4701-2（1995）	Environmental and durability testing methods for semiconductor devices Supplement 2) Solderability test and other revisions
ED-4701-3（1997）	Environmental and durability testing methods for semiconductor devices Supplement 3) ED-4701 revision
ED-4701-4（1998）	Environmental and durability testing methods for semiconductor devices Supplement 4) Soldering heat resistance test (SMD)
ED-4702（1992）	Mechanical strength testing methods for surface mounted semiconductor devices
ED-4703（1994）	Process internal evaluation and structural analysis methods for semiconductor devices
ED-4703-1（1995）	Process internal evaluation and structural analysis methods for semiconductor devices Supplement 1) Scanning acoustic tomography (SAT), etc.
EDX-4702（1994）	ESD breakdown testing methods for semiconductor devices (Preliminary) (Charged device model CDM/ESD)
EDR-4701B（1996）	Semiconductor device handling guide
EDR-4702（1996）	Semiconductor device quality and reliability testing method and standard comparison table
EDR-4703（1999）	Quality assurance guidelines for bare dies including KGD

KGD：Known Good Die

(3) JEDEC

JEDEC is equivalent to the U.S. Electronic Industries Alliance (EIA) division concerned with semiconductor devices, and both JEDEC and EIA are affiliated with the American National Standards Institute (ANSI).

JEDEC spans a wide range of fields including JESD22 which summarizes various environmental testing methods, JESD78 which describes latch-up testing methods, package outline specifications, packing magazine specifications, statistical process control (SPC), etc.

(4) Standards comparison table

Table 4-9 shows part of a table comparing the reliability testing methods of major standards (including Sony Semiconductor Network Company standards).

Table 4-9 Reliability Test Standards Comparison Table

<table>
<tr><th></th><th>Sony</th><th>EIAJ</th><th>IEC</th><th>JEDEC</th></tr>
<tr>
<td>Temperature cycle (Gaseous phase)</td>
<td>
• Condition selection (according to the product specifications)
A: –65±5 / 150±5°C
B: –55±5 / 125±5°C
C: –40±5 / 100 $^{+5}_{-3}$°C
D: –30±5 / 85 $^{+5}_{-3}$°C
E: –30±5 / 75 $^{+5}_{-3}$°C
F: 0 $^{+5}_{-3}$ / 125±5°C
G: –25±5 / 125±5°C

• High/low temperature exposure time
A to E: 30 minutes, F: 15 minutes, G: 10 minutes
• The shelf time includes the time from when the sample is placed in the chamber until the temperature inside the chamber stabilizes.
• Normal temperature exposure time
A to E: 5 $^{+0}_{-1}$minutes
FG: 2-zone test (automatic damper opening and closing)
• The condition G test temperature is prescribed by the sample temperature.
• A to F prescribe the temperature near the test area blow-out opening.
• Normal temperature (T_N): 5 to 45°C
• 100 cycles unless otherwise specified

• Continue and perform the soldering heat resistance test.

• Electrical characteristics measurement
</td>
<td>
EIAJ ED-4701-3 (1997)
Test method B-131A

• Tstg min~Tstg max
• Allowable temperature difference
125°C or more: ±5°C
Less than 125°C: $^{+5}_{-3}$°C
–25°C or more: $^{+5}_{-3}$°C
Less than –25°C: ±5°C
• Normal temperature (T_N): 5 to 35°C
• The shelf time is selected according to the sample discrete mass (m).
<table>
<tr><th>m (g)</th><th>a, c</th><th>b, d</th></tr>
<tr><td>m≦15g</td><td>10 minutes or more</td><td>5 minutes or less</td></tr>
<tr><td>15<m≦150</td><td>30 minutes or more</td><td>15 minutes or less</td></tr>
<tr><td>150<m≦1500</td><td>60 minutes or more</td><td>30 minutes or less</td></tr>
<tr><td>1500<m</td><td colspan="2">Prescribed individually</td></tr>
</table>
a: Low temperature shelf time
c: High temperature shelf time
b, d: Transition time

• Prescribed temperature arrival time: t
The longer of 5 minutes or 10% of a and c
• If the sample does not reach the storage temperature within the prescribed time, count the time from when the sample reaches thermal equilibrium.
• 5 cycles unless otherwise specified.
</td>
<td>
IEC60749 (1996-10)
CHAPTER 3 1.1

• Minimum storage temperature (°C) T_A
–65, –55, –40, –25, –10, –5, +5°C
±3°C in all cases
• Maximum storage temperature (°C) T_B
200, 175, 155, 125, 100, 85, 70, 55, 40, 30°C
±2°C in all cases
• Shelf time: t_1
10 minutes when the sample temperature reaches the prescribed temperature in 3 minutes or less, 10 minutes from when the sample temperature achieves equilibrium in all other cases.
(The sample temperature shall achieve equilibrium in 20 minutes or less, in any case.)
• Transition time: t_2
2 to 3 minutes or less (standard), 1 minute or less (automated equipment)
• 5 cycles
• The thermal time constants of the sample and carrier are taken into account.
• Electrical characteristics measurement + visual inspection of the exterior
• Air circulation speed inside the chamber: 2 m/s or more
• Absolute humidity inside the chamber: 20 g/m^3 or less
• The time from when the sample is placed in the chamber until the temperature inside the chamber stabilizes shall be included in the shelf time, but shall comprise 10% or less of the shelf time.

[Reference standards]
IEC60068-2-14(1984-01)
IEC60068-2-14-am1(1986-01)
</td>
<td>
JESD22-A104-A (1989)

• Condition selection
A: –55 $^{+0}_{-10}$ / 85 $^{+10}_{-0}$°C
B: –55 $^{+0}_{-10}$ / 125 $^{+10}_{-0}$°C
C: –65 $^{+0}_{-10}$ / 150 $^{+10}_{-0}$°C
D: –65 $^{+0}_{-10}$ / 200 $^{+10}_{-0}$°C
F: –65 $^{+0}_{-10}$ / 175 $^{+10}_{-0}$°C
G: –45 $^{+0}_{-10}$ / 125 $^{+10}_{-0}$°C
H: –55 $^{+0}_{-10}$ / 150 $^{+10}_{-0}$°C

• Normal temperature exposure is not prescribed.
• Transition time: 1 minute or less
• The load temperature shall arrive at the prescribed temperature in 15 minutes or less.
• Exposure time: 10 minutes or more each
• 10 cycles or more at condition C unless otherwise specified

• Acceptance test: 10 cycles
Certification test: 100 cycles
</td>
</tr>
</table>

Table 4-9 Reliability Test Standards Comparison Table

<table>
<tr><th></th><th>Sony</th><th>EIAJ</th><th>IEC</th><th>JEDEC</th></tr>
<tr>
<td>Thermal shock (Liquid phase)</td>
<td>
• –65±5～150±5℃
• GALDEN^{R} D02 TS
(Perfluoropolyether)
Electronics test grade used
• Dipping time: 5 $^{+1}_{-0}$ minutes
• Transition time: 10 s or less
• Standard 100 cycles
• Start from normal temperature and count from the low temperature side.

• Continue and perform the soldering heat resistance test.
</td>
<td>
EIAJ ED-4701-3 (1997)
Test method B-141A

• Temperature condition selection (Condition A unless otherwise specified)
A: 0 $^{+5}_{-0}$～100 $^{+0}_{-5}$℃ Fresh water (city water)
B: –55±5～125±5℃ Appropriate medium
C: –65±5～150±5℃
D: –200±5～150±5℃
E: $T_{stg\ max}$±5～$T_{stg\ min}$±5℃

• Condition divisions according to sample discrete mass
<table>
<tr><th></th><th>Over 1.5 kg</th><th>1.5 kg or less</th></tr>
<tr><td>Dipping time</td><td>5 minutes or more</td><td>15 s to 5 minutes</td></tr>
<tr><td>Transition time</td><td>10 s or less</td><td>3 s or less</td></tr>
</table>
• 10 cycles
• Start from normal temperature and count from the low temperature side.
</td>
<td>
IEC60749 (1996-10)
CHAPTER 3 1.2

• Temperature condition selection
(* unless otherwise specified)
0 $^{+2}_{-0}$～100 $^{+0}_{-5}$℃ *
–55～125℃
–65～150℃
–200～150℃
$T_{stg\ max}$～$T_{stg\ min}$℃

• Severity divisions
<table>
<tr><th></th><th>I</th><th>II</th></tr>
<tr><td>Dipping time</td><td>5 minutes to less than 20 minutes</td><td>15 s to less than 5 minutes</td></tr>
<tr><td>Transition time</td><td>8±2s</td><td>2±1s</td></tr>
</table>
• 10 cycles
• Start from normal temperature and count from the low temperature side.
</td>
<td>
JESD22-A106-A (1995)

• Temperature condition selection
(Condition C unless otherwise specified)
A: –40 $^{0}_{-30}$～85 $^{+10}_{-0}$℃
B: 0 $^{+2}_{-10}$～100 $^{+10}_{-2}$℃
C: –55 $^{+0}_{-10}$～125 $^{+10}_{-0}$℃
D: –65 $^{+0}_{-10}$～150 $^{+10}_{-0}$℃

• Perfluorocarbon
(Water for the high temperature side only of condition A)
• Liquid dipping time: 2 minutes or more
* The load shall reach the prescribed temperature in 5 minutes or less.
• Transition time: Less than 10 s
• The test shall not be interrupted during one cycle.
• If the number of interruptions is 10% or more of the total number of cycles, the test shall be repeated.
• 15 cycles at condition C
</td>
</tr>
</table>

Table 4-9 Reliability Test Standards Comparison Table

	Sony	EIAJ	IEC	JEDEC
Saturated Pressure Cooker Test (PCT)	121±3°C 100 $^{+0}_{-5}$%RH 2.0×10^5±10% Pa ¥ No bias ¥ Continue and perform the soldering heat resistance test. ¥ Test time: 96, 240, 504 h	N/A	N/A	JESD22-A102-B (1991) 121±1°C 100%RH 15±1 psig* ¥ No bias ¥ Endurance time A: 24 $^{+2}_{-0}$ h B: 48 $^{+2}_{-0}$ h C: 96 $^{+5}_{-0}$ h D: 168 $^{+5}_{-0}$ h E: 240 $^{+8}_{-0}$ h F: 336 $^{+8}_{-0}$ h *pounds per square inch 1psi=6895Pa 15psi=6895×15 =1.0×10^{5}Pa Standard atmospheric pressure 1atm=101325Pa ∴15psig=2.0×10^{5}Pa

Table 4-9 Reliability Test Standards Comparison Table

	Sony	EIAJ	IEC	JEDEC
Unsaturated Pressure Cooker Test	130±2℃ 85±5%RH 2.3×10^5 Pa • Continue and perform the soldering heat resistance test. • Voltage application (prescribed individually) • Test time: 200 h	EIAJ ED-4701-3 (1997) Test method B-123A • Condition selection A 110±2℃, 85±5%RH, 1.2×10^5 Pa B 120±2℃, 85±5%RH, 1.7×10^5 Pa C 130±2℃, 85±5%RH, 2.3×10^5 Pa • Voltage application if prescribed • Test time prescribed individually	IEC 60749 (1996-10) CHAPTER 3 4C • Condition selection Severity selection A 110±2℃, 85±5%RH, 1.2×10^5 Pa — 408h, 192h, 96h B 120±2℃, 85±5%RH, 1.7×10^5 Pa — 192h, 96h, 48h C 130±2℃, 85±5%RH, 2.3×10^5 Pa — 96h, 48h, 24h • Voltage application if prescribed	JESD22-A110-B (1999) Highly-Accelerated Temperature and Humidity Stress Test (HAST) • Condition selection 110±2℃, 85±5%RH, 1.2×10^5 Pa — 264^{+2}_{-0} h 130±2℃, 85±5%RH, 2.3×10^5 Pa — 96^{+2}_{-0} h • Power-on guidelines - Minimum power consumption - Apply to alternating pins as much as possible. - Apply a potential difference to the entire metal wiring. - Apply the maximum allowable voltage. - Continuous power-on when the thermal loss is 200 mW or less or when the die pad temperature rise is 10℃ or less. - Intermittent cycles at 50% duty (Power-on:Power-off = 1:1) - 1 cycle period t ≥ 2 mm: 2 h or less t < 2 mm: 30 minutes or less (t: package thickness) • The temperature and humidity until arrival at the test conditions are prescribed. • Measure within 48 h after placing in and removing from the chamber, and reapply stress within 96 h. The time provision is relaxed to 3 times for storage using bags to prevent the escape of humidity.

Table 4-9 Reliability Test Standards Comparison Table

	Sony	EIAJ	IEC	JEDEC
Soldering heat resistance (SMD) (IR reflow)	• Temperature provisions - Peak temperature: 260°C max - Preheating temperature: 170 ±10°C - Preheating time: 90 ±30 s • Baking + Moisturizing + Heating + Heating + Heating (3 times as standard) • Baking: 125 ±5°C for 24 h • Processing intervals Baking to moisture absorption: 5 minutes or less Moisture absorption to heating: 2 h or less Heating to moisture absorption: 3 h or less • Applicable only to moisture proof packaged products • The moisture absorption conditions are prescribed individually for each package. • Visual inspection of the exterior • Scanning acoustic tomography (SAT) • Cross section observation	EIAJ ED4701-4 (1998) Test method A-133B method I • Temperature provisions (including air reflow heating) I-A [- Peak temperature: 235 $^{+5}_{0}$ °C - Heating time: 10 ±3 s] ▲Sample volume less than 2,000 mm^3 I-B [- Peak temperature: 220 $^{+5}_{0}$ °C - Heating time: 10 ±3 s] ▲Sample volume 2,000 mm^3 or more • Preheating: 140 to 160°C for 90 ±30 s • Baking + Moisturizing + Heating + Heating (2 times as standard) (Moisturizing times upper limit: 3 times) • Processing intervals Moisture absorption to heating: 4 h or less Heating to heating: Until cooled to 50°C or less • Moisture absorption conditions 1) Moisture proof packaged products Perform moisture absorption in two stages during packed storage and after unpacking. The detailed conditions are as prescribed by each company. 2) Non-moisture proof packaged products A 85±2°C、65±5%RH、168±24h 〃 336±24h B 85±2°C、85±5%RH、168±24h • Visual inspection of the exterior • Scanning acoustic tomography (SAT) • Cross section observation • Electrical characteristics measurement	IEC60749 (1996-10) CHAPTER 2 2.3 • Temperature provisions - Peak temperature: 235 ±5°C - Heating time: 10 ±1 s - Preheating temperature: 150 ±10°C - Preheating time: 1 to 2 minutes (The temperature is the sample surface temperature.) • Baking + Moisturizing + Heating (IR reflow) • Baking: 125 ±5°C 6 h or more for baking at less than 125°C (The baking time at 125°C is not prescribed.) • Moisturizing conditions A 85°C30%RH 168h B 85°C65%RH 168h C 85°C85%RH 24h • Visual inspection of exterior + electrical characteristics measurement	EIA/JESD22-A-112-A (1995) • Temperature provisions - Peak temperature: 220 $^{+5}_{0}$°C - Heating time: 10 to 40 s (180°C or more for 120 to 180 s) - Temperature gradient: 6°C/s or less - Preheating temperature: 125 ±25°C - Preheating time: 2 minutes • Baking + Moisturizing + Heating + Heating • Baking: 125 $^{+5}_{0}$ °C for 24 h or more • Processing intervals Moisture absorption to heating: 15 minutes to 4 h Heating to heating: 5 minutes or more • Moisturizing conditions (susceptibility level divisions) 1) 85°C85%RH 168h 2) 85°C60%RH 168h 3) 30°C60%RH 192h 4) 30°C60%RH 96h 5) 30°C60%RH 72h 6) 30°C60%RH 48h 7) 30°C60%RH 6h • Visual inspection of the exterior • Scanning acoustic tomography (SAT) • Cross section observation • Electrical characteristics measurement