# Knowledge-Based Reliability Qualification Testing of Silicon Devices

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**Keywords:** Reliability Testing, Failure Testing, Failure Mechanisms

**Authors:** D.H. Eaton, N. Durrant, S.J. Huber, R. Blish, N. Lycoudes

**Approvals:** Noel Durrant, Program Manager
Dave Anderson, Director, Supplier Relations and Corporate Services
Dan McGowan, Technical Information Transfer Team Leader

# Knowledge-Based Reliability Qualification Testing of Silicon Devices

**D. H. Eaton, N. Durrant, S. J. Huber, R. Blish and N. Lycoudes**

**ABSTRACT**

Present day reliability qualification testing consists of a combination of stress-based testing and failure mode or knowledge-based testing. Each has its advantages and disadvantages. Effectively using a knowledge-based qualification testing approach requires considerable knowledge of the failure mechanism, its acceleration model and how to detect the particular failure mechanism as well as knowledge of the worst-case use conditions. In the realm of semiconductor device physics a knowledge-based approach has been used for many years in such areas as electromigration, hot carrier degradation, and gate oxide integrity. The approach is less mature in the area of semiconductor packaging for a variety of reasons. This paper describes the differences between stress-based and knowledge-based testing and the advantages and disadvantages of each. It also describes the information necessary in order to apply knowledge-based testing more broadly to semiconductor device and package reliability qualification.

## 1. Introduction

As the emphasis for decreasing costs and time to market in the semiconductor industry becomes even stronger, efficient and effective reliability qualification of products becomes more critical. Reliability qualification is often the last step before manufacturing release of a product and can thus directly impact time to market. Furthermore, the sample sizes and tests necessary to meet ever more stringent infant mortality and long-term reliability goals drive up the cost of qualification.

Silicon device reliability has been extensively studied and characterized. As a result, there are some well-accepted models for such failure mechanisms as hot carrier injection, gate dielectric breakdown, and electromigration. These failure mechanisms are often characterized and tested in advance of actual technology release. A somewhat different situation exists for IC packaging. Because the package types and materials are frequently changing, extensive characterization is not always possible and stress-based reliability tests are often performed on products shortly before manufacturing release. A migration from the direction of

stress-based to knowledge-based testing will, therefore, primarily affect package qualification.

Currently there are two JEDEC standards for the reliability qualification of silicon devices: JESD47—"Stress Test Driven Reliability Qualification of Silicon Devices" [1] and JESD34—"Failure-Mechanism-Driven Reliability Qualification of Silicon Devices." [2] This paper will address the similarities and differences of these two standards and suggest how the commonly practiced stress-based methodology for IC package qualification can evolve into more of a knowledge-based methodology.

## 2. Purpose of reliability qualification

The obvious purpose of doing a reliability qualification is to demonstrate fitness for use (i.e. reliability requirements have been met). Sometimes qualifications are used to estimate an upper bound on the incidence of field failures. Parts can fail in the field for a variety of generic reasons. For example:

- A fundamental wear-out mechanism of the part (silicon or package)
- Drift in a device parameter combined with a marginal design
- Latent manufacturing defects
- Manufacturing process excursions

Reliability qualification can address only some of these reasons for field failures. Since reliability qualification is a one-time event, it normally does not address things such as manufacturing process excursions or "maverick lots". Its main value is in the following:

- detecting fundamental wear-out mechanisms
- detecting design marginality combined with parameter drift
- determining failure rates due to latent manufacturing defects

The remainder of this paper addresses only these three purposes of reliability qualification.

## 3. History of stress-based reliability qualification for IC's

Stress-based qualification of IC's for commercial applications is embodied in JEDEC Standard JESD47, which had its beginnings with fundamental research into the failure mechanisms of semiconductors. Semiconductor specialists studying devices failing under normal use conditions for the purpose of reducing/eliminating these failures concluded that their studies would be facilitated if the failures could be reproduced in the laboratory and in shorter

period of time. The result was the development of accelerated testing. Much of the description and documentation of accelerated testing is found in the International Reliability Physics Symposium (IRPS) annual proceedings.

Military applications drove the need to compile these accelerated tests and qualification procedures for IC's and publish them in two specifications: MIL-STD-883 and MIL-M-38510. These testing standards evolved from the need to demonstrate that semiconductor components could perform acceptably under a wide variety of environmental conditions for the expected life of the product. When MIL-STD-883 was first issued it was highly controversial. There was some question as to whether the methods were too complex and expensive. However, as time went by the standard became more widely accepted. [3] By the early 1980's there was consensus in the market that passing the MIL-STD-883 tests would ensure adequate field reliability of the product in many applications. [4] Most semiconductor suppliers took the test requirements from these military specifications and incorporated them into their own internal reliability qualification processes. These internal documents and specifications prescribed which environmental stresses were required for certain changes in silicon fabrication, package assembly processes, or materials. Each company developed its own decision-making process to determine what changes required what qualification tests. The actual qualification test specifications were typically taken from the military specifications.

In the early 1990's the companies in JEDEC looked for alternative methods of performing qualifications and after extensive review developed JEDEC standard JESD34, "Failure-Mechanism-Driven Reliability Qualification of Silicon Devices." However the majority of practitioners continued to use the Mil-STD-883 for qualification. To provide a path towards alternative methods of qualification (i.e. Failure Mechanism based etc.), JEDEC published a modified version of the MIL-STD-883 qualification tests under the title "Stress-Test-Driven Qualification of Integrated Circuits" (JESD47). Publication of JESD47 allowed Stress Test Driven Qualifications to be influenced by commercial needs; it cautioned the user not to use stress tests indiscriminately but to consider the failure mechanisms as well, referring the reader to JESD34.

The stress-based reliability qualification methodology embodied in JESD47 and MIL-STD-883 has worked reasonably well for many generations of silicon and packaging technologies. But what are its strengths and its limitations?

## 4. Stress-based reliability qualification

### *4.1 Strengths of stress-based qualification*

Since the stress-based qualification methodology has been used for a long time, there is a wealth of data available regarding stress-based tests. Based on this information, customers can be reasonably certain that products which pass the prescribed stress tests in the MIL and JEDEC documents will perform with adequate reliability in nearly all field applications. These specifications also make it easier to apply a standard set of requirements to multiple suppliers and simplify the procurement process.

A second argument in favor of stress-based testing is that many of the tests are not arbitrary but are based on real environmental stresses. For example, thermal cycling is a stress that nearly all semiconductor products experience frequently during their operating life. The thermal cycling conditions defined by the military and JEDEC Standards seek to accelerate the field conditions and thus reduce the number of temperature cycles are needed. Similarly, bias/humidity stress is also a condition which many semiconductor products may experience, and the test conditions are designed to accelerate failures compared to field conditions.

Furthermore, every time a stress-based qualification test or reliability monitor test is carried out, additional data are generated that add to the knowledge base for that particular IC product and related technologies. Thus, each reliability test has the potential of providing information which can be leveraged in future qualifications.

Finally, another strength of stress-based qualification testing is that it is likely to detect interactions within the product. For example, a thermal cycling test may detect an interaction due to thermally induced stresses between the chip passivation and the package molding compound. Interactions like this might not be detected by tests that are focused on either the passivation or the molding compound.

### *4.2 Limitations of stress-based qualification*

In stress-based testing, the test requirements are quite rigid. For example JESD47 specifies 500 cycles of temperature cycling (TC) from –65 to +150$^{o}$C. Presumably this stress will provide reasonable assurance that the product will survive a “lifetime” of normal field thermal cycles. But either of these specification conditions used by itself does not take into consideration the failure mode or the acceleration factor for the thermal cycle test.

Using the 500-cycle stress as an example, if the acceleration factor between the TC stress conditions and field use conditions is 20, then passing 500 cycles of TC implies the part would survive 10,000 cycles under use conditions, which is 2 thermal cycles per day for 13.7 years. This may be a reasonable expectation for many products. However, if the acceleration factor were 80, then the product

would survive for 54.8 years, which may be well beyond the expected life of many products. In the latter case, the number of cycles in the TC stress test could be reduced substantially, saving time and money in qualification and reducing the package cost due to less stringent package design requirements.

A limitation of stress-based testing as it is presently applied, is that practitioners may not take into account 1) failure modes, models, and acceleration factors, and 2) expected field use conditions. Often this situation results from the fact that the specification is used like a prescriptive “cookbook” without consideration of the failure mechanisms. A person using JESD47 may just go to the table of tests without noting that Section 1.1 of the document states “This set of tests should not be used indiscriminately” and that potential failure mechanisms should be considered.

As a result of not considering the failure mechanisms, acceleration factors, and use conditions, the tests may be more severe or lengthy than actually required, as in the example given above. Also, there may be certain failure modes and field use conditions for which the stress-based tests are not severe enough. Such potential failure modes cannot be predicted without some knowledge of the failure mechanisms and the acceleration factors between the stress test condition and the use condition.

## 5. Knowledge-based reliability qualification

Knowledge-based qualification, also known as failure-mechanism driven reliability qualification, depends on having considerable information about reliability failure mechanisms and how they are accelerated. It was formally introduced by JEDEC in 1993 in Standard JESD34, “Failure-Mechanism Driven Reliability Qualification of Silicon Devices.”

One type of knowledge-based qualification test targets a specific failure mechanism. Once the failure mechanism is identified, a focused accelerated test is designed to detect that particular mechanism. A non failure specific (broad-band) reliability test such high temperature operating life (HTOL) may be capable of accelerating and detecting a large number of different failure mechanisms but is not necessarily efficient at detecting any one of them. By contrast, a specific, highly focused test such as that for electromigration uses specific test patterns and accelerated test conditions targeting appropriate metal lines to cause failures due to electromigration. The combination of this particular test pattern and specific environmental test conditions is very efficient at accelerating and detecting electromigration failures, but not good at detecting other types of reliability failures. Figure 1 schematically depicts a highly focused (high “Q”) test

for electromigration, indicating its highly peaked nature for detecting one particular failure mechanism.

### *5.1 Definition of Knowledge-based qualification*

Knowledge-based qualification is a methodology based upon detecting and understanding the specific failure mechanisms of a particular product. Once the failure mechanisms are known, accelerated tests designed specifically to detect those mechanisms are developed and applied. Implied in this qualification methodology is knowledge of

- -the failure modes and mechanisms, and the statistical distributions of failures
- -the acceleration models for the specific failure modes in the accelerated test
- -the field use conditions.

These three pieces of knowledge allow the accelerated test conditions to be chosen in such a way that passing the accelerated test ensures that the product will meet the field reliability objectives under the use conditions specified.

It should be pointed out that a key component of knowledge-based qualification is knowledge of the use conditions. Use conditions for semiconductor components vary widely. Therefore, the qualification must take into account the most severe use conditions to be encountered in the field. However, there are application segments for which parts may encounter only a narrow range of field conditions. An example is the Application Specific Integrated Circuit (ASIC) which is designed for one specific application or product. An ASIC which is used only in a mainframe computer which is kept in an air-conditioned environment and is turned off only rarely is one example. Such a part would not be subjected to nearly as many temperature cycles during its expected life as a part in a product which is cycled on and off daily. Such an ASIC is a good candidate for using knowledge-based qualification methods.

### *5.2 Developing a Knowledge-based qualification*

JESD34 contains an 8-step procedure to follow (section 5.5.2) in performing a failure-mechanism-based qualification. That section of JESD34 also lists the conditions under which generic data may be substituted for qualification test results on the actual product. The document specifies that all potential physical failure mechanisms be considered and that the field application use conditions be taken into consideration. It further states, “the supplier must validate that each of the baseline reliability qualification tests listed in Table I has been evaluated for its applicability to each qualification.”

Among the tests listed in Table I of JESD34 are:

Bias Life
High Temperature Storage Life
Accelerated Moisture Resistance—Unbiased Autoclave
Steady-State Temperature Humidity Bias
Electromigration
Electrostatic Discharge
Solderability
Temperature Cycling

The intent of the tests in Table I is to ensure that all potential failure mechanisms are considered and to ensure there is a bridge between the Failure Mechanism Based and Stress Test Driven qualifications. However if failure mechanisms are not properly considered, nothing is saved by using JESD34 instead of JESD47. The change from JESD47 to JESD34 alone will not automatically reduce costs and cycle times of qualifications. Proper application of knowledge-based qualification can reduce the qualification effort in two ways. 1) If it is determined that one of the above tests does not accelerate any known or potential failure mode of the device, then that test can be omitted. 2) Depending on the use conditions and acceleration factor, the test duration may be reduced from that prescribed by JESD47. However, in order to effectively use JESD-34 significant preparatory work is required, as will be discussed in later sections of this paper.

### *5.3 Types of knowledge-based qualifications*

Knowledge-based reliability qualifications can take a variety of forms. In some cases, a knowledge-based qualification can make use of a special device or test pattern which is optimized for detecting one particular type of failure mechanism. The test pattern used for electromigration mentioned earlier is an example. Another type of knowledge-based qualification may use the actual product and environmental tests very much like the tests in a stress-based qualification. In the latter case, the difference from a stress-based qualification is that the failure modes are known as well as the acceleration factors.

The following examples illustrate the characteristics of the types of knowledge-based qualifications.

### Type 1: Use of a specialized test device

An example of this type is aluminum electromigration. Electromigration testing has the following attributes.

a) A very specific set of failure modes

e.g. resistance increase due to aluminum voids; whisker growth between metal lines

b) Physical models for the failure modes

e.g. an understanding of mass transport of aluminum by electron flow

c) The distribution of failures due to this mechanism (e.g. lognormal distribution)

d) A verified mathematical model for the acceleration

e.g. Black's model [5] for aluminum voiding: time to failure ~ $J^{-n}[\exp(-E_a/kT)]$

(where T=absolute temperature; J=current density; n=an experimentally determined parameter; $E_a$= activation energy, an experimentally determined parameter; k=Boltzmann's constant)

e) Specific test devices which can measure failure due to electromigration and are insensitive to other failure modes

The electromigration testing is performed at higher values of T and J relative to the design-rule values in order to obtain acceleration. Since there is a verified acceleration model, the time-to-fail data can be accurately extrapolated to field use conditions.

Although this type of reliability testing is very valuable there are limitations. For example, the test patterns are not exactly like the metal lines on the actual product, although they are designed to replicate the actual geometries and topologies as much as possible. Any difference in failure mode or time to failure due to the differences between the test pattern and the actual product constitute a limitation of this type of knowledge-based testing. Consequently, making the test devices faithfully replicate the behavior of the actual product is key to successfully using the knowledge-based approach with specialized test devices.

**Type 2: Use of the actual product in the test**

As an illustration, consider the temperature cycle testing of a flip chip with solder bumps on a ceramic substrate using an actual product chip. The attributes of this particular test are

a. The failure modes are known

e.g. solder bump cracking and debonding

b. An approximate empirical acceleration model is known (here used in its simplest form for purposes of illustration):

Coffin-Manson model [6],[7]

Acceleration ~ $(\Delta T_{test}/\Delta T_{operating})^c$

where

$\Delta T_{test}$ is the temperature change during the accelerated test

$\Delta T_{operating}$ is the temperature change during operation
c is an experimentally determined constant (~ 1.9 for solder fatigue)

The advantage of using the actual product is that the physical dimensions and solder bump placement are those of the product, so no assumptions about extrapolating from a test device to the product are needed. A disadvantage is that there may be competing failure modes, so that time to failure must separated by failure mode before a statistical analysis can be done.

This Type 2 knowledge-based qualification may resemble stress-based qualification in that the traditional stress-based tests are done on actual product. However, an important difference from stress-based qualification is that with knowledge-based qualification the failure mechanisms and acceleration models are known. This fact permits the qualification engineer to use only those tests and test conditions (T, $\Delta T$, time, etc.) that assure the product will fulfill its intended field life. As we shall see later, this knowledge may permit modifying test conditions and reducing test times from those used in a stress-based qualification. It also allows us to quantify the reliability and lifetime of the device under particular field use conditions.

One concern about knowledge-based qualification is model accuracy. Most models depend on at least one experimental parameter, and there is variability in the data used to build the model. Therefore, any models must be appropriately guard banded when extrapolating results to field use conditions.

Figure 2 shows how the Coffin-Manson exponent varies with the exponent "c". For example, consider the line for which the $\Delta T$ ratio is 3 between accelerated test conditions and use conditions. (This $\Delta T$ corresponds to going from a temperature cycling test at $-65^{o}$C to$150^{o}$C to a use condition of $0^{o}$C to $72^{o}$C.) If the exponent c is known only to be in the interval 1.7 to 2.3, then the acceleration factor could vary from 6.5 to 12.5, about a factor of two. The conservative approach would use the lower acceleration factor when predicting the field lifetime from the accelerated test data.

Another way of looking at the effect of uncertainty in the data is to calculate the sensitivity of the acceleration factor to the Coffin-Manson exponent. This result is shown in Figure 3 for three different nominal values of c. It is seen that particularly for larger c, a small uncertainty in the exponent can lead to a considerable uncertainty in the calculated acceleration factor. A similar sensitivity analysis can be done around knowledge of the use conditions. Figure 4 shows the variation in acceleration factor as a function of variation in $\Delta T$. Since the use conditions typically are not precisely known, there will be a corresponding uncertainty in the Coffin-Manson acceleration factor.

This discussion points out the need to do “worst case” analysis and guard banding when using models to extrapolate accelerated test results to field use conditions. However, with appropriate guard banding, even imperfect knowledge can be used to advantage in establishing the appropriate stress test conditions. The empirical data and the model must correlate. If not, both the model assumptions and stress conditions should be investigated.

### *5.4 Knowledge necessary to perform a knowledge-based qualification*

Stress-based qualification is sometimes used (or misused) as a “cookbook.” In other words, you do the tests specified using the test conditions specified and if the test passes, you are covered. The relationship to use conditions is not considered. Alternatively, knowledge-based qualification endeavors to rely on engineering judgment to determine the proper tests and the appropriate test conditions to assure a given level of reliability under specified use conditions.

Thus, a successful knowledge-based qualification includes the following:

1. Knowledge of each failure mode or mechanism and the statistical failure distribution for the failure mode.

2. A reasonably accurate mathematical model which relates the accelerated test conditions to the field use conditions.

3. Knowledge of the field use conditions in which the product will be used. For example:
   - Temperature of the device when operating
   - Extremes of temperature cycling range
   - Frequency of temperature cycling
   - Ambient humidity at the device and range of humidity
   - Frequency of power cycling
   - Duty cycle
   - Customer’s expected useful life of the product

In addition, if the qualification testing is performed on test devices rather than on actual product, two additional pieces of information are needed.

4. A test device that is very good at detecting the failure mode of interest but is relatively insensitive to other failure modes

5. A method of assuring that failure modes due to interactions are detected

It should be noted that considerable up-front work must be done whenever new materials or structures are introduced to determine the failure modes and the

acceleration models (1 and 2 above). This work can be both expensive and time-consuming. For a new technology using new materials, it is critical to identify all possible failure modes and mechanisms. Utilization of a quasi stress-based approach is warranted here as a "stress to fail" method may be appropriate. Once the fail modes and mechanisms are identified, model development begins. If knowledge-based qualification is to be used effectively, the failure modes and acceleration models should be developed concurrently with the technology development. This approach will allow the qualification testing and analysis to proceed without undue delay for model development.

### *5.5 Advantages of knowledge-based qualification*

When the knowledge of failure mechanisms and acceleration factors and appropriate test patterns are available, knowledge-based qualifications have several advantages over stress-based qualifications.

First, fewer parts are needed for completing the qualification, saving time and money. Presumably if the failure mode is known and the acceleration models are well known, one would have to test only enough parts to show with good statistical confidence that the failure mode will not appear during the field life of the part. In most cases, this number of parts will be considerably below the 231 parts required for many of the JESD47 tests. For example, once the parameters of Black's equation for electromigration have been determined for a particular technology, only 30-50 parts are generally needed to qualify a new metal deposition process for electromigration. Since the failure distribution for electromigration failures is known to be lognormal, a curve fitted to the failure data provides the basis for predictive modeling.

A second advantage is elimination of long qualification tests, thus decreasing the time to market. This decrease in test time is dependent on knowing the acceleration models and the field use conditions. Presently reliability qualification testing is often the limiting factor in releasing to production new silicon or packaging technologies or a new product, so reducing the length of the longest tests is very important. As an example, consider a failure mode accelerated by storage at high temperature such as wire bond degradation due to intermetallics, contamination or voiding [8]. If this is the major failure mode which a high temperature storage test will detect for a new wire bonding process or material set, knowledge of the acceleration factor (based on the Arrhenius model) and the operating temperature during use can be used to advantage. The standard high temperature storage test is 6 weeks (1000 hours); in many cases this is the longest test for package qualifications. But if the activation energy and worst-case use conditions are known accurately, it may be possible to reduce the duration of the test by a considerable amount.

For example, suppose we know that wire bond failure times follow the Arrhenius equation [ Time to failure ~ $\exp(-E_a/kT)$ ]. Assume also that the activation energy ($E_a$) for this failure mechanism is known to be 1.1eV, +-0.1eV and that the worst-case maximum junction temperature of the device is 75$^o$C. Then, assuming $E_{a.}$ = 1.0 eV, the minimum acceleration factor for a 150$^o$C high temperature storage (HTS) test is 369. The standard 1000-hour HTS test is thus equivalent to 369,000 hours (42 years) at 100% duty cycle at worst-case operating temperature. If it were desired to test to a 20-year life, the HTS test may be reduced to 476 hours, saving over 3 weeks in qualification time. This example, of course, assumes that we know the statistical distribution of failures in time and that the sample size is sufficient to assure the desired wire bond reliability at the end of life.

A third advantage is better prediction of field reliability than is possible with stress-based testing. This feature allows suppliers to be better equipped to answer customer questions about field reliability under a variety of field use conditions. Furthermore, understanding the failure modes of the devices can accelerate improvements in silicon technology and package design to reduce or eliminate those failure modes and thus further improve reliability.

### *5.6 Limitations of knowledge-based qualification*

While knowledge-based qualification can have significant advantages in terms of cost and cycle time, there are some dangers and limitations which should be recognized.

Incomplete knowledge can lead to incomplete reliability testing. As mentioned previously, some knowledge-based qualifications use a specially designed test structure optimized to detect a specific failure mechanism. Such test structures typically aren't designed to detect interactions between different parts of the product. For example, a test structure and measurement designed to specifically measure gate oxide breakdown on capacitors may not detect gate oxide damage due to subsequent processing (process-induced damage). If prior knowledge of process-induced damage did not exist, a suite of knowledge-based qualification tests might not include a test for this phenomenon, and it would be overlooked.

Another potential shortcoming is relating reliability results on test structures to the reliability of the actual product. If the environmental aging process of the test structure is different from that of the actual product, care must be taken that the extrapolation to the actual product is valid. This extrapolation can be different than simply the acceleration factor of the environmental test and lead to over or underestimate of the reliability impact.

For instance, hot carrier degradation testing is typically done in a DC mode on minimum-length FET's under worst-case hot carrier accelerated stress conditions (maximum Vdd and Vg=~1/2 Vdd). However the circuit is operated under AC conditions, and in a digital circuit, the worst-case hot carrier degradation occurs only during a small period of time during switching. In order to relate the DC hot carrier results to actual circuit operation, appropriate models and simulations are required. An example is the Berkeley Reliability Tool (BERT) [9] which predicts the aging of FET's which will occur under actual circuit operation and then uses the degraded FET models to simulate the speed performance of the circuit. Without such models and simulation tools, the hot carrier specification may be overly conservative, and unnecessarily limit circuit performance.

Finally, the effectiveness of knowledge-based qualifications is only as good as the knowledge you have. If you don't have knowledge of a particular failure mode, then it is unlikely that you will include a test for it in the knowledge-based qualification. It is important to do a thorough analysis of potential failure modes at the beginning of the testing program and to include any tests that might even have a remote possibility of revealing a failure mode.

## 6. Present use of knowledge-based qualification

Knowledge-based qualification is presently being used extensively in the semiconductor industry. Nearly all the silicon device physics reliability tests for gate oxide integrity, hot carrier, and electromigration are knowledge based. Each of these phenomena has an adequate physical and acceleration model. These models are modified as more knowledge is gained, but the basic premise that a test device can be measured and the measurements extrapolated to product with enough confidence to assure adequate reliability throughout the life of the product. One reason that the models are so well understood and developed is that silicon, silicon dioxide, aluminum/copper, and FET technology have been used for many years and these materials and devices have been very well characterized. We are now challenged to quickly achieve a similar level of understanding of high dielectric constant gate dielectrics, copper metallization, and low dielectric constant interlayer insulators.

While knowledge-based qualification is common for silicon device and interconnect technology, such is not the case for semiconductor packaging technology. Some of the reasons are

- Incomplete physical understanding of failure mechanisms such as interface delamination
- Package configurations and materials are changing too rapidly to become well characterized before becoming obsolete

- More variability in packaging materials and interfaces than in silicon device materials

More extensive implementation of knowledge-based qualification is dependent upon developing a more thorough understanding of packaging materials and interfaces and to achieve better process control in the packaging arena.

A promising approach for gaining a package knowledge base is finite element analysis (FEA) of stresses in current and proposed packages. If materials properties are known with sufficient accuracy, FEA can be effective in understanding likely failure modes and locations. It can also be used to determine the worst-case package geometries. If the worst cases undergo and pass reliability qualification tests, then packages with lower stresses may be able to be qualified with a reduced set of tests.

## 7. Future direction of knowledge-based qualification

The industry is presently using a combination of stress-based and knowledge-based qualification. Most qualification test plans conform to the JESD47 document and the test conditions conform to the environmental conditions referenced there. However, in many instances the acceleration models for the environmental tests are known. Thus the accelerated test results can actually be used to estimate field reliability and time to wear-out rather than just to claim that the test has been "passed". Furthermore both JEDEC and SEMATECH have begun work on documents which support and specify conditions for doing application specific semiconductor qualifications and the associated acceleration models. [10],[11],[12],[13] These documents contain information on many failure mechanisms as well as their acceleration models and associated constants. The models are well accepted for silicon devices and interconnect since these technologies utilize a relatively stable set of well-understood materials. However for packages, the list of failure mechanisms and acceleration models is not complete, because materials are rapidly changing as packaging technologies evolve. Thus, the development of appropriate failure mode and acceleration models is critical prior to undertaking a qualification involving a new package type. The same caution applies if new materials (e.g. copper, low k dielectrics) are introduced into a silicon technology. Reference 11, "Use Condition Based Reliability Evaluation of New Package Technologies," contains an approach to performing qualifications when a new material is involved.

To evolve from the present state of stress-based qualification of packages, with limited understanding of failure mechanisms and acceleration models, to true knowledge-based qualification will require a concerted effort. Understanding of materials properties (such as modulus, coefficient of thermal expansion, strength,

and fracture toughness) and interface adhesion properties might best be done through university research. Industry or industry consortia can work on better specifications for materials and for better process control of materials and packaging/assembly processes. The motivation for doing this work is the cost and time to market improvements which can be achieved through knowledge-based qualification.

## 8. Summary

While stress-based testing has strong historical precedence, this form of testing, as typically practiced, does not always take into account specific failure mechanisms or field use conditions. Furthermore, there is the chance of overstressing some materials, causing spurious failures, using the standard stress-based tests.

Knowledge-based testing takes into account 1) the specific failure mechanism and failure distribution; 2) the acceleration factor in going from test conditions to use conditions; and 3) the actual field use conditions. In order to successfully implement knowledge-based testing, one must have knowledge of these three items. Knowledge-based testing often uses specialized test devices which are optimized for detecting a particular failure mechanism. When using such devices, it is important to have a model which correlates the results on the test device with the failures on actual product. A limitation of using test devices instead of actual products is in the detection of interactions between process steps or between the silicon device and the package.

The industry is presently using a combination of stress-based and knowledge-based testing. The primary application of knowledge-based testing is in silicon device reliability; package reliability testing is still largely stress based. In order to move package reliability qualification testing to knowledge-based testing, a better fundamental understanding of package materials properties, interface properties, failure mechanisms, and acceleration factors is needed. Only when such knowledge and models are in place can true knowledge-based qualification be achieved. There is a strong motivation in the industry to move from stress-based reliability testing to knowledge-based testing in order to reduce costs, shorten time to market, and enhance customer satisfaction

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D. H. Eaton is with Agilent Technologies, Fort Collins, Colorado
N. Durrant is with Intel Corporation and on assignment at SEMATECH, Austin, Texas
S. J. Huber is with Intel Corporation, Chandler, Arizona
R. Blish is with Advanced Micro Devices, Sunnyvale, California
N. Lycoudes is with Motorola, Chandler, Arizona

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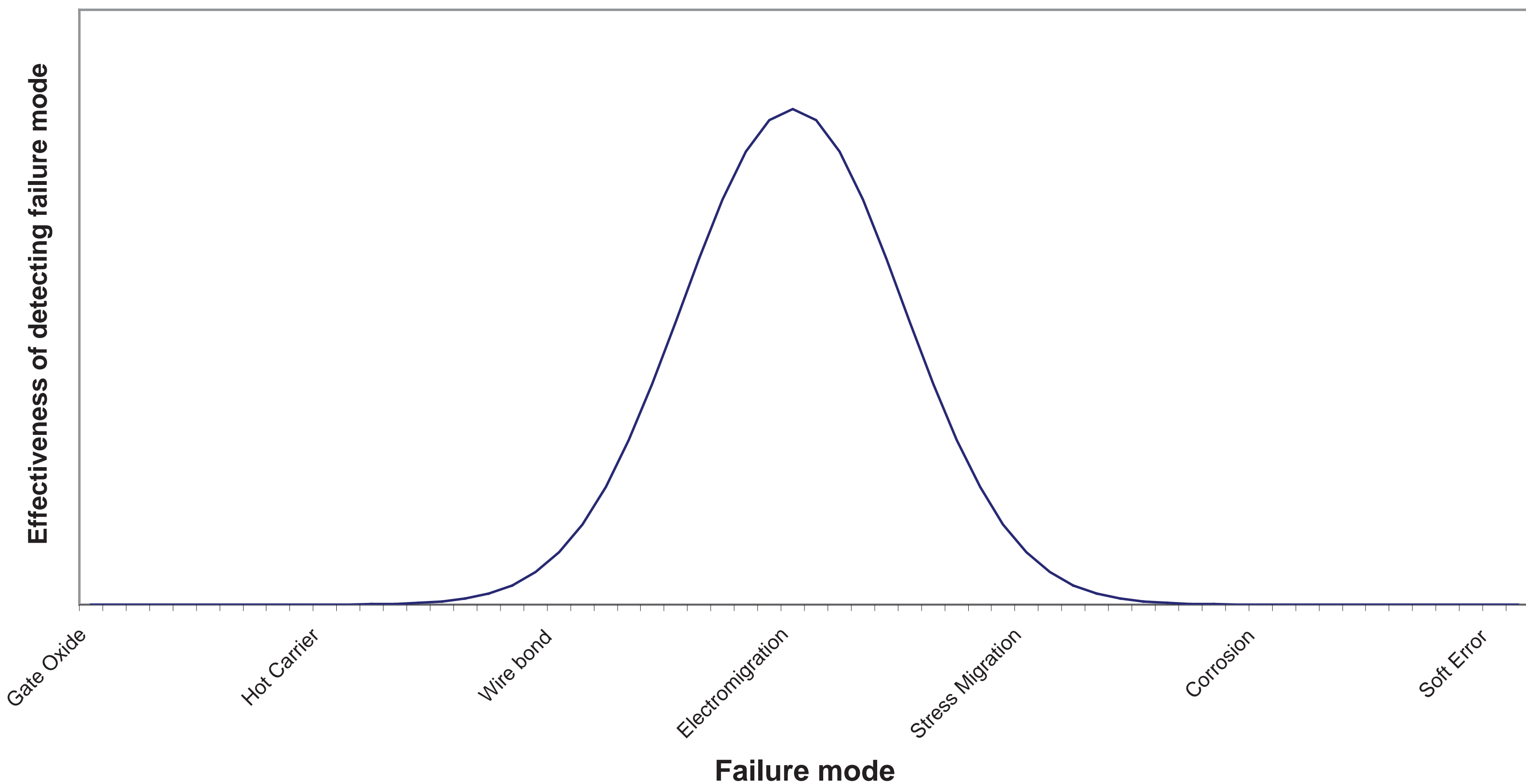


Figure 1

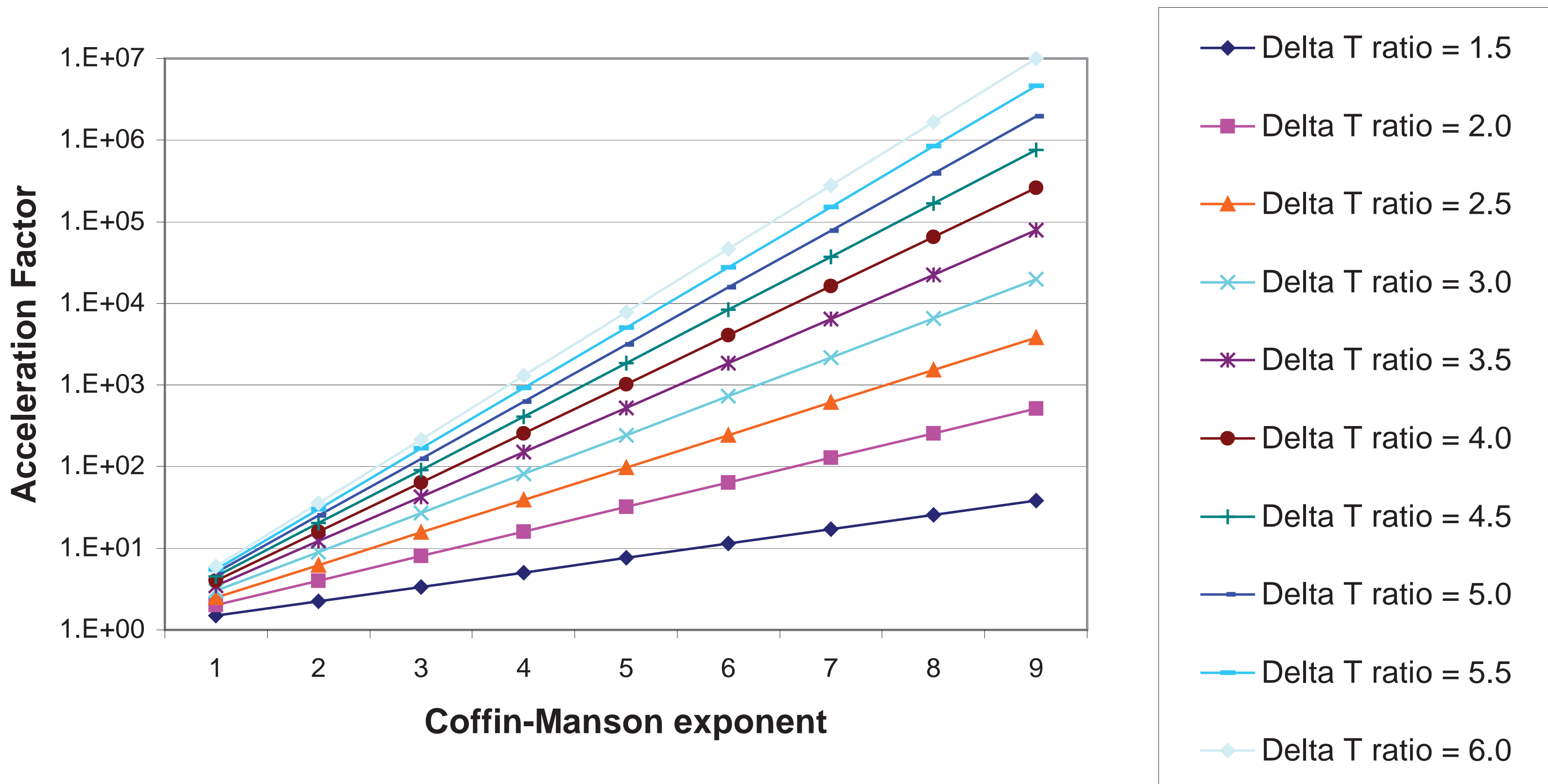


Figure 2

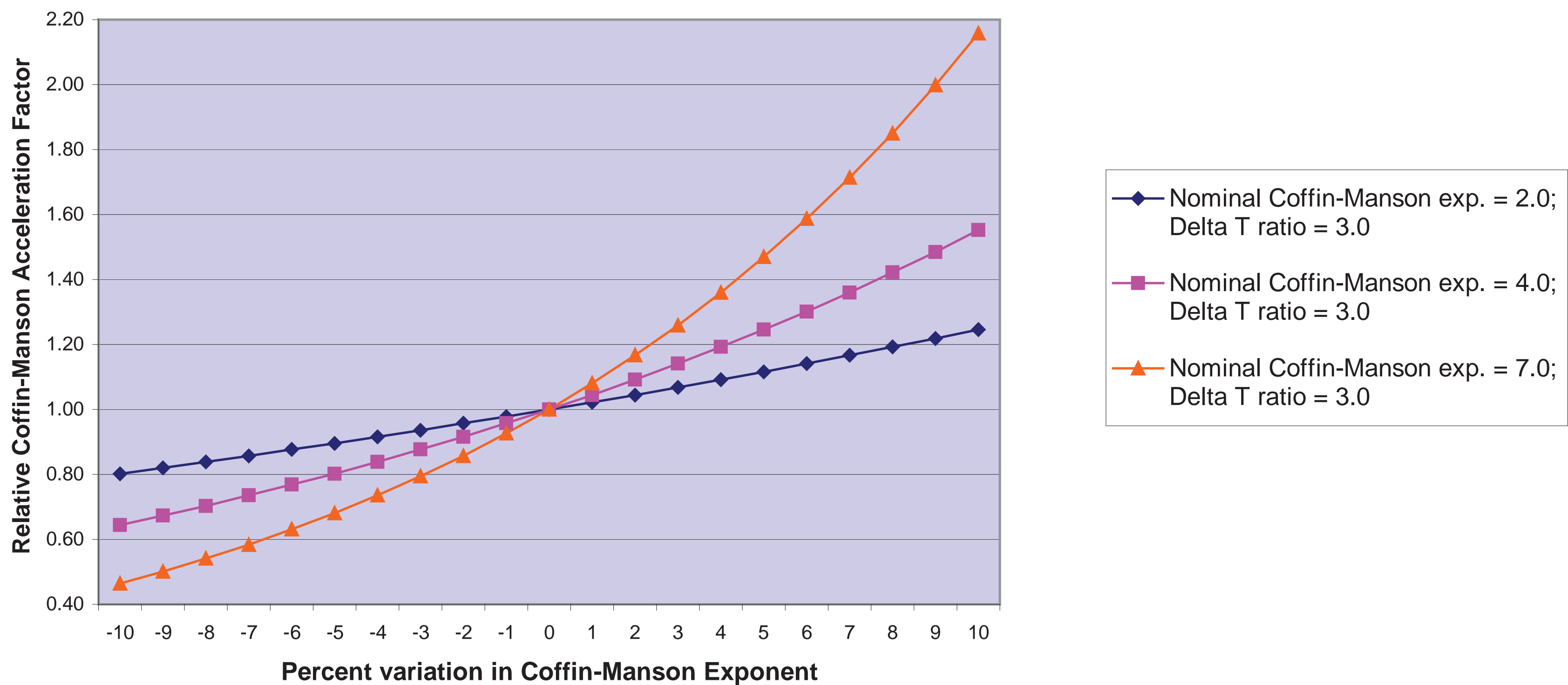


Figure 3

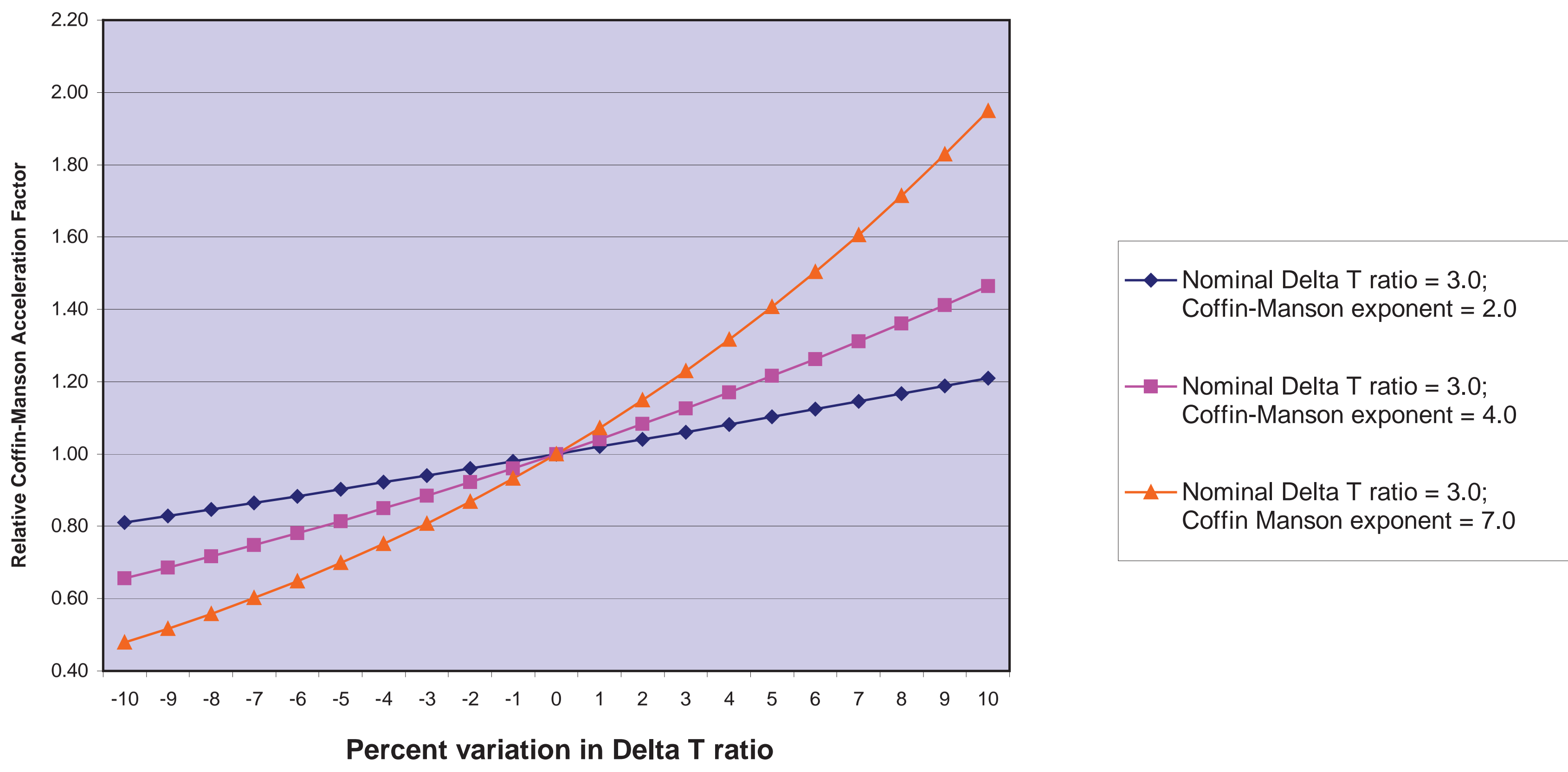


Figure 4

**International SEMATECH Technology Transfer**
**2706 Montopolis Drive**
**Austin, TX 78741**

**http://www.sematech.org**
**e-mail: info@sematech.org**