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Application Specific Qualification Using Knowledge Based Test Methodology

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APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY

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APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY

Introduction

The solid state component industry manufactures devices that are used in a wide range of applications. Consequently, the accelerated stress portion of the qualification regimen used to assess the reliability performance of these devices should be customized to match the range of end use applications, based upon knowledge of the customer's end use application conditions, environment, life time requirements, potential failure mechanisms, and associated failure models. The practice of using prescribed reliability stress test conditions, durations, sample sizes, and acceptance criteria may be inappropriate, especially with the ever-evolving applications and material sets found in the solid state component industry. The historically prescribed stress tests may either produce false failures or not accelerate valid failure mechanisms because the stress conditions do not correlate appropriately to the actual use environment.

APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY

(From JEDEC Board Ballot JCB-08-40, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

The method described in this document applies to all application specific reliability testing for solid state components with known failure mechanisms where the test duration and conditions vary based on application variables. This document does not cover reliability tests that are characterization based or essentially go / no-go type tests, for example, ESD, latch-up, or electrical over stress. Also, it does not attempt to cover every failure mechanism or test environment, but does provide a methodology that can be extended to other failure mechanisms and test environments.

The purpose of this document is to provide a method for developing an application specific reliability evaluation methodology based on the use conditions the solid state device is expected to experience in the field. It assumes that the failure mechanisms and models, relevant to the product being tested, are a known entity.

2 Terms and definitions

acceleration factor (*A,* AF): For a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition

NOTE 1 Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

NOTE 2 Acceleration factors can be calculated for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

NOTE 3 Acceleration factors are a function of one or more of the basic stresses that can cause one or more failure mechanisms. For example, a plot of the natural log of the time-to-failure for a cumulative constant percentage failed (e.g., 50%) at multiple stress temperatures as a function of $1/kT$, the reciprocal of the product of Boltzmann's constant in electronvolts per kelvin and the absolute temperature in kelvin, is linear if one and only one failure mechanism is involved. The best-fit linear slope is equal to the apparent activation energy in electronvolts.

NOTE 4 The abbreviation AF is often used instead of the symbol *A*.

2 Terms and definitions (cont'd)

environmental relative humidity: The relative humidity in the area immediately surrounding a specified component in an application.

environmental temperature cycle: A temperature cycle in an application resulting from environmental temperature changes.

environmental temperature range: The temperature range found in the area or enclosure surrounding an application.

field lifetime: (1) The anticipated time a product will last in the field determined solely by its ability to function.
(2) The anticipated time a product will be in use in the field determined by need rather than by its ability to function.

minicycle: A temperature cycle in an application resulting from a small degree of change in the operational temperatures (e.g., due to PC program variations).

nonoperating lifetime: The length of time that a component is not operating in an application.

NOTE The nonoperating lifetime may be calculated by subtracting the power-on-hours (POH) from the field lifetime.

operating lifetime: The length of time that a component is expected to function in an application at or below the predicted failure rate, stated in power-on-hours (POH).

operating temperature cycle range: The temperature range of a component caused by power cycling.

power cycle: A temperature cycle in an application resulting from cycling power on and off.

NOTE The hibernate, shutdown, and standby modes are classified as power off.

shipping environment: The temperature and relative humidity to which a component is exposed while being shipped.

shock and vibration condition: The shock and vibration experienced by an application in manufacturing, shipment, operation, and user handling (user transportation and/or regular operation).

storage environment: The temperature and relative humidity to which a component is exposed while being stored in a nonoperating state.

2 Terms and definitions (cont'd)

storage lifetime: The length of time that a component is in storage prior to usage in an application.

use conditions: The environmental factors during manufacturing, shipping, and useful life to which a component is exposed.

NOTE The useful life consists of the operating, nonoperating, and storage lifetimes.

3 References

JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices.*

JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components.*

JESD85, *Calculation of Failure Rate in Units of FITs.*

JESD91, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms*.

JESD22-A110, *Highly Accelerated Temperature and Humidity Stress Test (HAST)*.

JESD22-A118, *Accelerated Moisture Resistance-Unbiased HAST*.

JESD22-A102, *Accelerated Moisture Resistance-Unbiased Autoclave*.

JESD22-A101, *Steady-State Temperature Humidity Bias Life Test*.

JESD22-A103, *High Temperature Storage Life*.

JEP131, *Process Failure Modes and Effect Analysis (FMEA)*.

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*.

JEP143, *Solid State Reliability Assessment and Qualification Methodologies*.

JEP148, *Reliability Qualification of Semiconductor Devices based on Physics of Failure and Risk and Opportunity Assessment*.

SEMATECH White Paper #99083810A-XFR, *Use Condition Based Reliability Evaluation of New Semiconductor Technologies*.

SEMATECH White Paper #99083813A-XFR, *Use Condition Based Reliability Evaluation: An Example Applied to Ball Grid Array (BGA) Packages*.

4 Determining application specific test requirements

It is necessary to determine the range of use conditions the solid state device will experience in the application space(s). This information can be obtained from customer requirements or based on general knowledge of the typical use, operation and reliability requirements for the product's market segment.

4.1 Identification of environmental, lifetime and manufacturing conditions

Key information required to develop an application specific qualification test sequence are the environmental, lifetime and manufacturing conditions to which the solid state device will be exposed. Dependent on the application and the failure mechanism of interest, only some of these attributes may play a critical role in the customization of the test sequence. With this in mind, the criteria that shall be given consideration for the intended application include, but are not limited to:

- expected operating lifetime of the device in power-on hours
- actual number of weekly operating hours
- device operating voltage and electric field
- number of environmental and power cycles experienced per day
- number of mini-cycles and sleep cycles per day, if applicable
- ambient relative humidity and temperature range of the environment where the device operates
- storage conditions (temperature and humidity)
- shipping conditions (temperature, humidity and shock / vibration)
- expected assembly layout and assembly conditions (pwb cross section, heat sink attachment, surrounding devices, reflow profile)
- cumulative end of life failure rate
- early life failure rate

5 Identification of potential failure modes

Expected failure modes can be identified in several ways, but one of the most effective is to perform a failure mode and effect analysis (FMEA) on the product of interest, see JEP131. Another method that can be used in conjunction with performing an FMEA is the modeling of the product. Based on its design and material attributes, the model can predict any thermal or mechanical interactions in the application environment, which could initiate stresses and associated product failure.

5 Identification of potential failure modes (cont'd)

If unknown failure mechanisms are found during test, appropriate acceleration model experiments need to be designed and performed in order to establish models, activation energy and test duration. JESD91, Method of Developing Acceleration Models for Electronic Component Failure Mechanisms, describes how to accomplish this task.

6 Selection of failure modes for known failure mechanisms

Once the potential known failure modes and mechanisms are identified, the appropriate failure models should be selected. Appropriate models and activation energies for the range of known failure mechanisms are discussed in JEP122, Failure Mechanisms and Models for Silicon Semiconductor Devices.

7 Selection of test hardware

Test hardware shall be representative of the expected application design with respect to key attributes, yet capable of discerning stress test failures. These include, but are not limited to, expected component layout, circuit board cross-section, and heat sink requirements. For the most representative test results, the test hardware build should simulate the anticipated manufacturing assembly, test, burn-in and shipping conditions. The test hardware may be either actual product or test vehicles designed to simulate product attributes. Dependent on the failure modes and mechanisms of concern, a test vehicle may be preferable since the actual product complexity may mask intrinsic failure mechanisms. A valid test hardware strategy should take this into account.

8 Selection of stress tests

Stress tests shall be selected based on the expected failure modes. JESD47, Failure Mechanisms and Models for Silicon Semiconductor Devices relates many process attributes and the accelerated tests used to stress solid state device attributes to failure. JEP 122 and JEP143 have extensive information on various reliability stress testing models, concepts and methods. The duration of the testing is dependent on the range of the applications' space.

9 Selection of stress test conditions and durations

Stress test conditions and associated preconditioning shall be selected that accelerate the failure mode of interest, but do not produce false failure modes that are artifacts of the test conditions and not representative of the product's use environment. Selection must be based on solid state device material properties versus use conditions and test acceleration factors. The reliability stress conditions should be bounded so that they are not beyond the physical capability of the product materials. These physical limits may dictate upper and/or lower limits on the stress conditions selected. If the actual use condition requirements are beyond the physical limits of the product materials, testing should be performed at those limits to demonstrate product incompatibility for the specific application. Material properties of interest include, but are not limited to, coefficient of thermal expansion, modulus and elongation as a function of temperature and creep properties. The test duration shall be based on the failure model selected, the acceleration factor for that mechanism, the failure rates that need to be verified for the product, including early life and end of life. It should be noted that if the acceleration factor is small for the failure mechanism of interest, the test time could be long. If the test duration is unreasonable, alternative stress test conditions or methods should be explored. The test intensity shall be derived from environmental and operation conditions, and be designed within stated limits of material and capability of test hardware. The sample size used needs to be sufficient to support the failure rate requirements. JESD74, Early Life Failure Rate Calculation Procedure for Electronic Components, and JESD85, Calculation of Failure Rate in Units of FITs are the applicable documents for failure rate and distribution determination, based on stress test results. If the failure rate requirement is low, the quantity of parts tested could be large. The test sequence should simulate the handling, shipping and use conditions for the application, and as such, combination of tests may be warranted.

9.1 Selection thermal cycle test conditions

Thermal cycle test conditions, in particular, must be selected with care. The selection of the thermal cycle range and duration for the stress test should be based on the use environment for the product, life of the product and constituents of the product being stress tested. These cautions are discussed in JESD22-A104, Temperature Cycling.

In either development or qualification, several thermal cycle conditions can be performed on the product. Ideally parts should be stressed to a preselected failure percentage. Failure modes should be compared between thermal cycle conditions. It is critical that all failure mechanisms encountered be judged against use conditions for the intended product. Failures observed at the most severe conditions may not represent a field concern for that application and are merely an artifact of the severe test conditions. These can include failures generated by extreme thermal cycling which exceeds the material's glass transition temperature, moisture absorption by the carrier and material ductility at low temperatures.

9 Selection of stress test conditions and durations (cont'd)

9.1 Selection thermal cycle test conditions (cont'd)

Exceeding the glass transition (t_g) of a material changes the coefficient of thermal expansion, as well as, the properties of the given material. Exceeding the ductility of materials can generate unrealistic failures due to brittleness and crack propagation at the lower temperature exposures.

9.2 Selection of temperature/ humidity (with and without bias) stress conditions

HAST and autoclave testing, while being useful development tools, must be used with caution since these stress conditions and duration can cause degradation of package materials which will lead to unrealistic failure of the package with respect to the application environment. From an organic package perspective, over stressing in temperature / humidity with or with out bias can lead to the following type of problems:

- excessive package delamination inconsistent with field application conditions
- excessive corrosion and metal migration inconsistent with field environment
- temperature and humidity effects that will not be seen in the field application

These concerns are discussed in the following temperature and humidity test methods:

JESD22-A110, Highly Accelerated Temperature and Humidity Stress Test (HAST), JESD22-A118, Accelerated Moisture Resistance-Unbiased HAST, JESD22-A102, Accelerated Moisture Resistance-Unbiased Autoclave, and JESD22-A101, Steady-State Temperature Humidity Bias Life Test.

9.3 Selection of thermal aging stress conditions

The cautions related to this stress condition are exceeding the material t_g and material interface adhesion. Extended exposure of organic packages to high temperatures result in oxidation and breakdown of the organic materials and can adversely affect mechanical and electrical performance of the package. JESD22-A103, High Temperature Storage Life, discusses this test method.

9.4 Selection of stress voltage conditions

The precautions related to this stress condition are the application of voltages or transients exceeding the oxide or junction breakdown voltage(s) or excessive ramp rates which could permanently destroy or adversely affect the electrical performance of the device.

9 Selection of stress test conditions and durations (cont'd)

9.5 Selection of other stress conditions

As with specific test conditions discussed above, the same level of caution should be applied when selecting the specific test limits for any accelerated test chosen to be performed in the application specific test sequence. See the various JEDEC test methods for guidance.

10 Establish product performance

Perform the use condition qualification stress tests based on the application requirements. Collect the reliability stress test data. The test results must be analyzed to determine if the product meets or exceeds the application requirements, including end of life failure expectations. The test sample size and test failures are important variables in failure rate determination see JESD85, Calculation of Failure Rate in Units of FITs. Failure mechanisms must be reviewed to rule out failures that are not consistent with field conditions and failures that are relevant to the field, but occur beyond the end of life for the application space. The latter can occur when failure mechanisms, with a range of activation energies, are present in the test samples. If the parts tested are too complex, unlayering of root cause for the test failures may be very difficult or impossible. As such, this concern should be taken into account when the test hardware is designed or selected.

11 Applying application specific test methodology

Examples of the application specific test methodology are included in the Annex that follows. The examples demonstrate how different application use conditions require varied test durations. It should be noted that the application conditions listed in the examples are for the tutorial purpose of demonstrating how to apply the knowledge based test methodology and should not be construed as absolute use conditions for a specific market segment. The test sequence is also an example and not intended to prescribe a specific reliability test sequence.

Annex A (informative) Application specific methodology

A.1 Application use condition comparison

Table 1 lists examples of several key application conditions for a number of product applications. The specific application condition data is for illustrative purposes only and should not be construed as an absolute for any product type. Actual application conditions should be determined based on data collected at the intended application, in coordination with the user, if possible. Other application conditions, such as shipping, storage or handling shall be considered, based on the application performance requirements. The type of use condition information listed in Table 1 should be available for specific products or applications. Dependent on the failure mechanism of interest, different reliability test sequences will be selected. The pertinent application information needed to perform a knowledge based test sequence will depend on the failure model of interest. The failure model can also have a range of activation energies or coefficients that are dependent on the failure mechanism of interest. Prior to selecting specific models and attributes, the user should have a good understanding of the application and the subtleties of the applicable models.

Annex A (informative) Application specific methodology (cont'd)

Table 1 — Illustrative application conditions (examples only) for a range of applications

Applications	Application Conditions								
	Transport/ handling dynamic events	Operating Life (POH)	Field Lifetime (Years)	Environmental & Power Cycles	Environmental Relative Humidity Range (% RH)	Environmental Temperature Range (°C)	Operational Temperature Cycle Range (°C)	Chip Junction Temperature (Tj) Typical/ Max. (°C)	Device Nominal Operating Voltage (V)
Desk Top Computer with Enrgy Saving Features	Shipping	13,000*	5 years	Main: 1/ day Mini: 17/ day Short: 1/ day	10- 80%	10° – 30°C	Main: 20° – 60°C Mini: 52° – 60 °C Short : 40° – 60 °C	70°C / 105°C	12.0 V
High End Server	Shipping	94,000*	11 years	4 / year	10 – 80%	10° – 30°C	14° - 55°C	70°C / 105°C	1.2 V
Avionic Electronincs in Cockpit	Shipping	>150,000*	~ 23 years	Power: 21,500 2.5 / day	5 – 80%	-20° – 50°C	0° – 50°C	70°C / 105°C	3.3V/ 5V
Telecom Hand Held	Shipping / User handling	43,800*	5 years	Talk: 20 / day Standby/ Off: 1/ day	10 – 95%	-40° - 40°C	Talk: 32° - 70°C Standby/ Off: 30° - 32°C	30°C / 70°C	1.8V / 3.3V
Telecom Uncontrolled	Shipping	131,000*	15 years	Power: 1/ month Environ: 1/ day	85%	-40° - 85°C	Power: Δ 85°C Environ: Δ 25°C	85°C / 110°C	1.2 V
Telecom Controlled	Shipping	131,000*	15 years	Power: 1/ month Environ: 1/ day	70%	0° - 70°C	Power: Δ 85°C Environ: Δ 6°C	85°C / 110°C	1.2 V
Automotive Underhood (Grade 0)	Shipping / User handling	8200*	15 years	Power: 5 / day	0 – 100%	-40° - 125°C	-40° - 150°C	100°C / 150°C	12.0 V

*** POH value assumes worst case 100% power-on over the life of the application. Actual application use POH may be less.**

A.2 Accelerated thermal cycle comparison

Table 2 lists the number of temperature cycles needed to verify solder joint integrity for the application conditions listed in Table 1. As can be seen, dependent on the application, a wide range in the number of temperature cycles required for verification is evident. The number of cycles for solder joint fatigue is found by applying a failure model appropriate for this failure mechanism. In this case, the Norris-Landzberg modification of the Coffin-Manson model was selected, see Equation 1. This modification of the Coffin-Manson approach adds additional multiplicative terms relevant to solder joint fatigue. The factors are a cyclic frequency factor as a power law (exponent used in this example is 1/3) and a mild Arrhenius-like temperature dependence (using an approximation of the Arrhenius thermal activation of exp (0.01 $T_{stress} - T_{field}$). It should be noted that by using this approximation temperatures can be expressed in either °C or K. The acceleration factor due to environmental test sequence assumes an exponent for solder strain of 1.9. For the example, two cycles per hour (48 cycles per day) is the test condition and the frequency of cycling for the field per day is assumed to be at 6 or greater (see JESD22-A104). In this example, all system frequencies, except for the computer mini cycles, fall below the 6 cycles/ day value. Thus for the calculations, 6 cycles/ day were assumed for the remaining application cycles. Three different temperature cycle test conditions are listed. This comparison is provided to demonstrate that dependent on the temperature cycle range selected, the test duration can vary significantly. It should be noted that selection of the harshest condition might not be acceptable for the material set found in a specific application. Acceleration factors can be modulated by material property and test configuration; hence it is recommended that appropriate evaluation is conducted to determine applicability of those parameters.

Shown below is a solution to the Norris Landzberg equation using the high end server application conditions found in Table 1.

Equation 1: Norris-Landzberg Modification of the Coffin-Manson Equation

$$AF = (\Delta T_{stress} / \Delta T_{field})^{1.9} (\nu_{field} / \nu_{stress})^{1/3} e^{0.01(T_{max\ stress} - T_{max\ field})}$$

ΔT_{stress} = 100 °C
ΔT_{field} = 41 °C
ν_{field} = 6 *
ν_{stress} = 48
$T_{max\ stress}$ = 100 °C
$T_{max\ field}$ = 55 °C

Solving the equation for the high end server application conditions, AF = 4.27 test cycle equivalent to end of life = (# Cycles/ life) / AF = (4/ year x 11 years)/ 4.27 = 9 cycles of 0° – 100 °C thermal cycling needed to verify solder joint integrity for the application example.

Annex A (informative) Application specific methodology (cont'd)

Table 2 — Temperature cycling accelertion factors and test cycles for various applications

Applications	Acceleration Factor (AF) / Application Test Cycles		
	Temperature Cycling Test Conditions JESD22-A104		
	Condition B (-55° - 125°C)	Condition G (-40° - 125°C)	Condition J (0° - 100°C)
Desk Top Computer with **Enrgy Saving Features**	Main: AF 16.69 / 109 cycles Mini: AF 355.15 / 87 cycles Short: AF 62.28 / 29 cycles TOTAL CYCLES: 225	Main: AF 14.14 / 129 cycles Mini: AF 301 / 103 cycles Short: AF 52.79 / 35 cycles TOTAL CYCLES: 267	Main: AF 4.25 / 429 cycles Mini: AF 128.1 / 242 cycles Short: AF 15.88 / 115 cycles TOTAL CYCLES: 786
High End Server	AF 16.74 / 3 cycles	AF 14.19 / 3 cycles	AF 4.27/ 9 cycles
Avionic Electronincs in Cockpit	AF 12.07/ 1781 cycles	AF 10.23 / 2102 cycles	AF 3.08 / 6981 cycles
Telecom Hand Held	Talk: AF 24.9/ 1466 cycles Standby/ Off AF 6545/ 0.28 cycles TOTAL CYCLES: 1467	Talk: AF 21.1/ 1730 cycles Standby/ Off: AF 5548/ 0.33 cycles TOTAL CYCLES: 1731	Talk: AF 6.3/ 5759 cycles Standby/ Off: AF 1669/ 1 cycles TOTAL CYCLES: 5760
Telecom Uncontrolled	Power: AF 3.10 / 58 cycles Environ: AF 31.74 / 172 cycles TOTAL CYCLES : 230	Power: AF 2.63/ 68 cycles Environ: AF 26.9/ 204 cycles TOTAL CYCLES : 272	Power: AF 0.79/ 228 cycles Environ: AF 8.09/ 677 cycles TOTAL CYCLES : 905
Telecom Controlled	Power: AF 3.10/ 58 cycles Environ: AF 477.8/ 11 cycles TOTAL CYCLES : 69	Power: AF 2.63/ 68 cycles Environ: AF 405/ 14 cycles TOTAL CYCLES : 82	Power: AF 0.79/ 228 cycles Environ: AF 121.8/ 45 cycles TOTAL CYCLES : 273
Automotive Underhood (Grade 0)	AF 0.35/ 78,000 cycles	AF 0.30/ 91,000 cycles	AF 0.09/ 300,000 cycles

Annex A (informative) Application specific methodology (cont'd)

A.3 Accelerated temperature, humidity and bias example

This example will illustrate the methodology for calculating the acceleration factors and stress duration for Temperature Humidity and Bias Stress. The HAST stress per JESD22-A110, will be employed to demonstrate the methodology for the Aluminum corrosion failure mechanism for the application conditions listed in Table 1. Dependent on the application and conditions, a wide range in stress durations are possible, as shown in Table 5.

The Peck power law model is used for the Aluminum corrosion failure mechanism (ref. JEDEC Publication No. 122):

$$TF = A_o \cdot RH^{-N} \cdot f(V) \cdot e^{\frac{E_a}{kT}} \qquad (1)$$

where:

- A_o = scale factor
- RH = $RH_{diesurface}$ = Relative Humidity (%) at die surface
- N = 2.7 – 3.0
- E_a = 0.7 – 1.0 eV
- f(V) = function of applied voltage

The Relative Humidity at the die surface ($RH_{diesurface}$) in equilibrium is calculated using the following relationships, from C.G. Shirley, The Reliability Models and Life Prediction for Intermittently-Powered Non-Hermetic Components, Proceedings of IRPS-1994, pg. 72.

$$P_{sat}(T) = e^{(a + \frac{b}{T} + \frac{c}{T^2} + \frac{d}{T^3})} \qquad (2)$$

where:

- a = 16.0332248
- b = -3515.13806
- c = -290850.583
- d = 5097236.05
- T = Temperature in K

NOTE P_{sat} can be obtained also from a standard reference table.

and

$$RH_{diesurface} = RH_{amb} \cdot \frac{P_{sat}(T_{amb})}{P_{sat}(T_{diesurface})} \qquad (3)$$

Annex A (informative) Application specific methodology (cont'd)

For the Telecom Hand Held application, the rise in the I.C. junction temperature, ΔT_j, is calculated for the various operating conditions:

$$\Delta T_j\ (^\circ C) = \text{Power Dissipation x Package Thermal Impedance} = PD \times \theta_{ja} \quad (4)$$

For this example, it is assumed that $T_{ambient,application}$ = 30 °C and $RH_{application}$ = 70%. The $P_{sat(Tamb)}$ and $P_{sat(Tdiesurface)}$ are calculated using equation (2). $RH_{diesurface}$ is calculated using equation (3). The results of these calculations are shown in Table 3.

Table 3 — Calculations results for operating modes and conditions

	Operating Mode		
	Talk	**Standby**	**Shutdown**
T_{amb} (°C)	30	30	30
ΔT_j (°C)	40	2	0
$T_{diesurface}$ (°C)	70	32	30
$P_{sat(Tamb)}$	4.3	4.3	4.3
$P_{sat(Tdiesurface)}$	31.2	4.8	4.3
RH_{amb}(%)	70	70	70
RH_{chip}(%)	9.6	62.5	70

The HAST stress environmental condition is 130 °C/85% RH. The power dissipation of the product during HAST stress is minimized so that the $RH_{diesurface}$ ~ $RH_{HAST\ ambient}$. In addition, f(V) is assumed to be 1 since the same bias conditions used in the application are applied to the product in the HAST stress. The acceleration factor for HAST stress can be calculated by equation (1). Two different sets of values for N and Ea are used in the example for comparative purposes. The moisture saturation time for the package is assumed to be 24 hours for HAST. The saturation time for application ambient is neglected. The equivalent stress time for each mode is calculated by:

$$t_{HAST} = t_{sat,HAST} + \frac{Total_Time_in_Life}{AF} \quad (5)$$

where:

$$\frac{\text{Total Time in Life}}{\text{AF}} = \text{HAST Stress Time with Bias}$$

Annex A (informative) Application specific methodology (cont'd)

The HAST stress time is calculated for a 10 year product lifetime at an average ambient temperature of 30°C and Relative Humidity of 70%.

Table 4 — Acceleration Factors for HAST stress for Application with Ambient at 30ºC and 70% Relative Humidity

HAST Acceleration Factors and Durations										
Application Life			**HAST Acceleration (N = 2.66, Ea = 0.79 eV)**				**HAST Acceleration (N = 3.0, Ea = 0.9 eV)**			
Operating Mode	**Usage per Day (Hrs)**	**Total Life Usage (Hrs)**	**AF_{HAST}**	**Pkg. Saturation $t_{SAT,HAST}$ (Hrs)**	**HAST Stress Time (Hrs)**	**HAST Total Duration (Hrs)**	**AF_{HAST}**	**Pkg. Saturation No Bias $t_{SAT,HAST}$ (Hrs)**	**HAST Stress Time With Bias (Hrs)**	**HAST Total Duration (Hrs)**
Talk	2	7,300	17,902	24	0.2	24.2	64,500	24	0.1	24.1
Standby	14	51,100	3,383	-	7.6	7.6	10,391	-	2.5	2.5
Shutdown	8	29,200	3,047	-	4.8	4.8	9,255	-	1.6	1.6
Total HAST Duration (Hours of Continuous Stress)				**24**	**13**	**37**		**24**	**4**	**28**

For the above example, approximately 32 to 49 hours of HAST, depending on the activation energy, Ea, and exponent N, is needed to demonstrate the equivalent use time in the Telecom Hand Held application. Acceleration factors for other environmental conditions and for other applications can be calculated similarly.

Annex A (informative) Application specific methodology (cont'd)

Table 5 — Temperature and humidity acceleration factors and stress duration for various applications and use conditions

THB and HAST Acceleration Factors and Stress Durations for Various Applications and Use Conditions				
Application	**Operational Mode**	**Average Envirnomental Condition Tamb (ºC) / Rhamb (%)**	**THB JESD22-A101-B (85ºC / 85% RH)** (N =2.66, Ea = 0.79 eV)	**HAST JESD22-A110-B (130ºC / 85% RH)** (N =2.66, Ea = 0.79 eV)
Desk Top Computer with Enrgy Saving Features	Main: Mini Short: Shutdown: Package Saturation **Total Stress Time:**	40ºC / 65% 56ºC / 65% 50ºC / 65% 25ºC / 65%	AF 287 / 41.8 hrs AF 59 / 8.5 hrs AF 105 / 4.8 hrs AF 354 / 87.1 hrs 24 hrs **166 hrs**	AF 5010 / 2.4 hrs AF 1025 / 0.5 hrs AF 1855 / 0.3 hrs AF 6134 / 5.0 hrs 24 hrs **32 hrs**
High End Server	Main: Package Saturation **Total Stress Time:**	25ºC / 65%	AF 2722 / 34.5 hrs 24 hrs **59 hrs**	AF 47,466 / 2.0 hrs 24 hrs **26 hrs**
Avionic Electronincs in Cockpit	Main: Shutdown: Package Saturation **Total Stress Time:**	35ºC / 65% 30ºC / 65%	AF 843 / 177.9 hrs AF 598 / 83.7 hrs 24 hrs **286 hrs**	AF 14,701 / 10.2 hrs AF 10,418 / 4.8 hrs 24 hrs **39 hrs**
Telecom Hand Held Application	Talk: Standby: Shutdown: Package Saturation **Total Stress Time:**	30ºC / 70% 30ºC / 70% 30ºC / 70%	AF 1027 / 3.6hrs AF 194 / 131.7 hrs AF 175 / 83.6 hrs 24 hrs **243 hrs**	AF 17,902 / 0.2 hrs AF 3,383 / 7.6 hrs AF 3,047 / 4.8 hrs 24 hrs **37 hrs**
Telecom Uncontrolled	Main: AF Shutdown Package Saturation **Total Stress Time:**	45ºC / 85% 35ºC / 85%	AF 84 / 1556.6 hrs AF 64 / 6.3 hrs 24 hrs **1587 hrs**	AF 1,467 / 89.3 hrs AF 1,113 / 0.4 hrs 24 hrs **114 hrs**
Telecom Controlled	Main: AF Shutdown Package Saturation **Total Stress Time:**	35ºC / 70% 25ºC / 70%	AF 402 / 325.9 hrs AF 290 / 1.4 hrs 24 hrs **351 hrs**	AF 7,008 / 18.7 hrs AF 5,061 / 0.1 hrs 24 hrs **43 hrs**
Automotive Underhood (Grade 0)	Power-On Power-Off Package Saturation **Total Stress Time:**	75ºC / 75% 15ºC / 75%	AF 6.5 / 1261.9 hrs AF 703 / 175.3 hrs 24 hrs **1461 hrs**	AF 113 / 72.4 hrs AF 12,255 / 10.1 hrs 24 hrs **107 hrs**

Annex B (informative) Differences between JESD94A and JESD94.01

This table briefly describes most of the changes made to entries that appear in this standard, JESD94A, compared to its predecessor, JESD94.01 (May 2007). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	Description of change
2	Updated terms and definition for consistency.
9	Updated clause with addition of preconditioning statement based on application.
Annex A	Table 2 calculations were updated.

B.1 (informative) Differences between JESD94.01 and JESD94

Clause	Description of change
3	Reference to JESD34 was removed, the document was rescinded in November 2004 and no longer applies.
3	Reference to JESD90 (5th on list): The document number listed, JESD90, was incorrect, and was changed to JESD91.
3	Reference to JESD47 (12th on list): The document title listed for JESD47, *Failure Mechanisms and Models for Silicon Semiconductor Devices*, was incorrect, and was changed to: *Stress-Test-Driven Qualification of Integrated Circuits.*

Standard Improvement Form JEDEC **JESD94A**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:
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   - ☐ Test method number ______ Clause number ____________

   The referenced clause number has proven to be:
   ☐ Unclear ☐ Too Rigid ☐ In Error

   ☐ Other ________________________________

2. Recommendations for correction:

____
____
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3. Other suggestions for document improvement:

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